UM7108 Series

One Chip 3 1/2-Digit Digital Multimeter

Features

- Multi-function measurement system:
  - Analog to digital converter
  - Data hold and Peak hold, both with LCD annunciators
  - Short circuit beeper with LCD annunciator
  - Low battery detector with LCD annunciator
  - Frequency counter with two LCD annunciators (UM7108F)
- Frequency counter: Auto range from 2 KHz to 20 MHz
- Triplex LCD display
  - Full 3 1/2-Digit Display
  - 6 annunciators — Data-hold, Peak-hold, KHz, MHz, Low-bat, Continuance
  - 1 annunciator drive pin for unit display
  - 3 decimal point drivers with 3 independent control pins
  - Polarity driver
  - Displays "OL" for input overrange
- Provides serial data output for other applications (UM7108F)
- Guaranteed zero reading with zero input
- True polarity indication for precision null detection
- Convenient 9V battery operation
- Low power operation — 10mW
- Low noise A/D converter
  - Low noise — 15 μV
  - Differential inputs — 1 pA bias current
  - Differential reference for ratiometric ohms
  - On-chip voltage reference — 20 ppM/°C drift
  - Low linearity error guaranteed less than 1 count
  - High Impedance CMOS differential inputs —$10^{12}\Omega$
- Applications: digital panel meters, digital multi meters, thermometers, capacitance meters, pH meters, photometers etc.

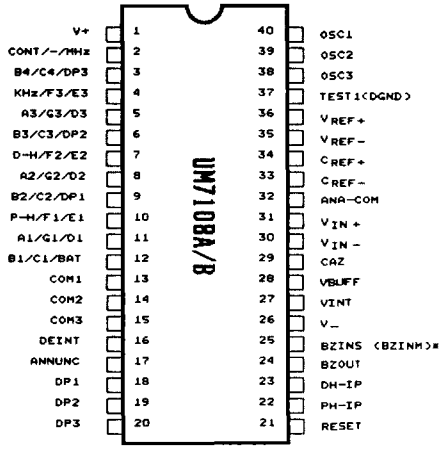
General Description

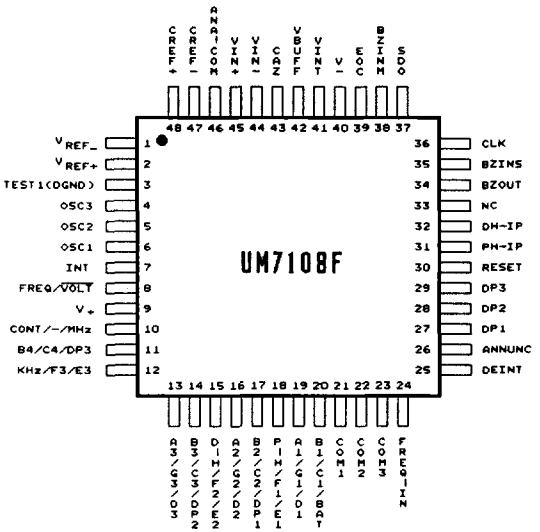
The UM7108 is a one chip 3 1/2-Digit Digital Multimeter which combines an integrated A/D converter , peak-hold, data-hold, short circuit beeper and low battery detector in a 40-pin DIP. The UM7108F 48-pin QFP includes a frequency counter, and serial data output.
In UM7108, an autozero cycle guarantees a zero reading with a 0 Volt input. CMOS structure reduces analog input bias current to only 1 pA and low power consumption. Rollover error is less than 1 count. Differential reference inputs permit ratiometric measurements for resistor or bridge transducer applications.

A 'PEAK-HOLD' input allows the UM7108 to hold the highest A/D readout. This feature is useful in measuring the starting current of motors, maximum temperatures and similar applications. However, the 'DATA-HOLD' input allows the UM7108 to hold the current A/D readout or frequency readout. This feature is useful in measuring unstable measurements or in preventing abnormal inputs which may confuse the measurements.

The frequency counter is auto ranging from 2 KHz to 20 MHz over a five decade range with KHz and MHz annunciators, which are useful in measuring normal frequencies.
Short circuit beeper will sound whenever the readout is less than 30 after enabling the short circuit beeper. This feature is useful in detecting short circuits without watching the LCD.
The UM7108 provides 3 independent decimal point driving pins for the manufacturer to determine which decimal point is displayed. The 3 decimal point drivers are built-in in UM7108. The UM7108 also provides one annunciator pin for manufacturer to easily display the unit on LCD. With the above features, the total system cost of a 3 1/2-digit digital multimeter will be reduced by using UM7108. The UM7108 operates from a 9 volt battery, same as UM7106, with typical power of 10 mW; and the packages include 40-pin DIP and 48-pin quad flat pack.

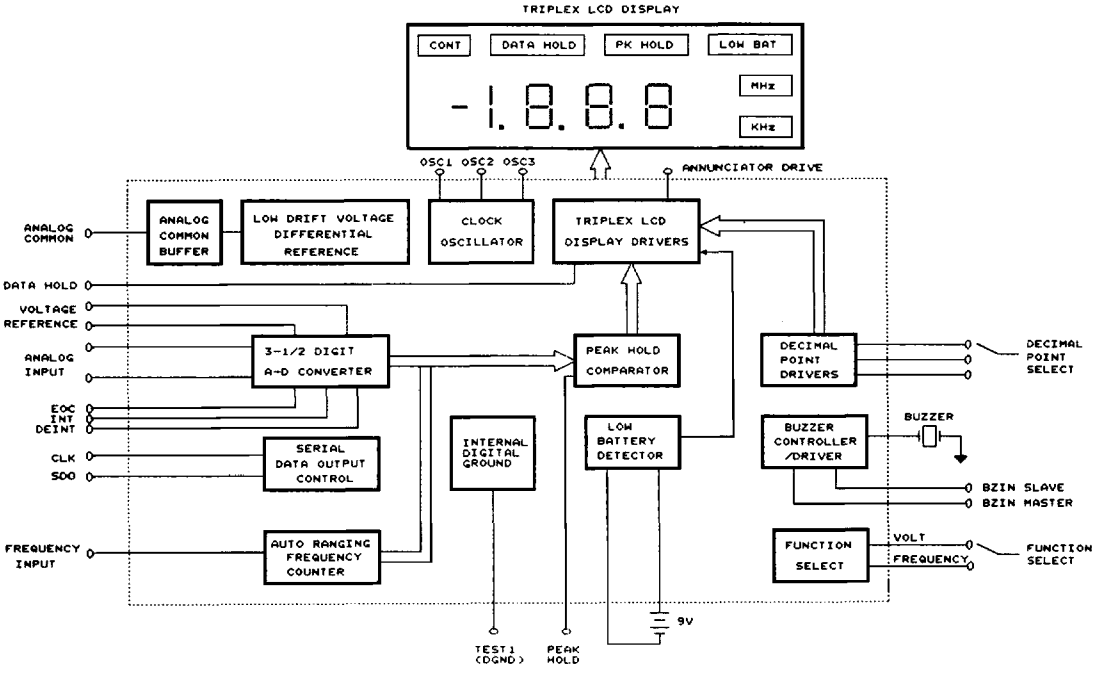
Pin Configurations





* Note: Pin 25 [BZINS— UM7108A
BZINM— UM7107B

Block Diagram



Absolute Maximum Ratings*

Supply Voltage (V+ to V-) 15V
Analog Input Voltage (either input) . . . ..V+ to V-
Reference Input Voltage (either input) . ...V+ to V-
Clock Input . . . . . Test to V+
Power Dissipation 800mW
Operating Temperature . . . . . .0°C to + 70°C
Storage Temperature . . . .–55°C to + 150°C
Lead Temperature (Soldering, 10 sec) . . . . ..260°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Unless otherwise noted, specifications apply to UM7108 at Vsupply (V+ to V-) = 9.0V, T_A = 25°C, Fclock = 40 KHz

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Zero input Reading	–	-000.0	±000.0	+000.0	Digital Reading	Vin = 0.0V Full Scale = 200.0mV
Ratiometric Reading	–	999	999/ 1000	1000	Digital Reading	Vin = Vref Vref = 100.0mV
Linearity (Max. Deviation From Best Straight Line Fit)	–	–1	±0.2	+1	Counts	Full Scale 200.0 mV or 2.000V
Noise	V_N	–	15	–	μV	Vin = 0V Full Scale 200.0mV
Leakage Current Input	I_{LEAK}	–	1	10	pA	Vin = 0V
Zero Reading Drift	–	–	0.2	1	μV/°C	Vin = 0V 0° < T_A < 70°C
Scale Factor Temp Coeff	–	–	1	5	ppm/°C	Vin = 199.0mV 0° < T_A < 70°C
Analog Common Voltage (With Respect to Positive Supply)	$V_{ANA-COM}$	2.8	3.0	3.2	V	25KΩ Between Common and Positive Supply
Temp Coeff of Analog Common	–	–	20	50	ppm/°C	25KΩ Between Common and Pos Supply
Common-mode Rejection Ratio	– –	– –	50	200	μV/V	Vcm =±1V, Vin = 0V Full-scale = 200.0mV

DC Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Current (Doesn't include LCD and Com. Current)	I_{DD}	–	1.2	1.8	mA	Is (Vin = 0.0V)
LCD Pk-Pk Segment Drive Voltage	V_{LCDS}	4	5	6	V	
LCD Pk-Pk Back Plane Drive Voltage	V_{LCDS}	4	5	6	V	
Rollover Error	–	-1	±0.2	+1	Counts	Vin+ = Vin- = 200.0mV
Frequency counter input level	V_{FRE}	V+ – 1.0	–	–	V	Vih(FREQ)
		–	–	DGND+1.0	V	Vil(FREQ)
Low battery margin	V_{LOW}	6.7	7.2	7.7	V	(between V+ to V-)
Input terminal: BZINM, BZINS, PH-IP, DH-IP, RESET, FREQ/ VOLT, CLK, DP1, DP2, DP3						
Input logic low voltage	V_{il}	–	–	DGND+1.5	V	
Input logic high voltage	V_{ih}	V+ – 1.5	–	–	V	
Pull down current	I_{pd}	–	5	–	μA	Vin = V+
Output terminal: EOC, SDO, INT, DEINT						
Output logic low voltage	V_{OL}	DGND	–	DGND+0.5	V	
Output logic high voltage	V_{OH}	V+ – 0.5	–	V+	V	

AC Characteristics

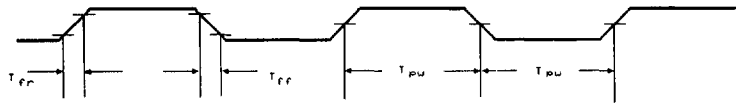
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Peak-hold duration	T_{ph}	0.8	–	–	sec	
PH-IP and DH-IP Keys						
Key debounce time	T_{deb}	–	32	38	ms	
Key hold time	T_{dh}	50	–	–	ms	

AC Characteristics (continued)

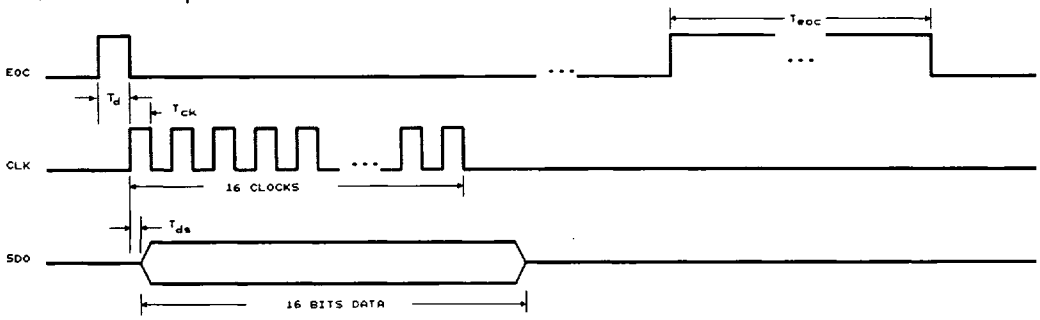
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
LCD display frequency	Flcd	–	167	–	Hz	
Operating frequency	Fclock	–	40	–	KHz	
Buzzer drive frequency	Fbzout	–	2.5	–	KHz	
FREQ-IN Waveform Rising Time	Tfr	–	–	20	ns	
FREQ-IN Waveform Falling Time	Tff	–	–	20	ns	
FREQ-IN Waveform Pulse Width	Tpw	17	–	–	ns	
Clock Delay Time	Td	1	–	5000	μs	
Data Set-up Time	Tds	–	–	500	ns	
EOC Pulse Width	Teoc	–	–	10	ms	
Clock Pulse Width	Tck	500	–	–	ns	

Timing Waveforms

1. Frequency Counter Input Waveform

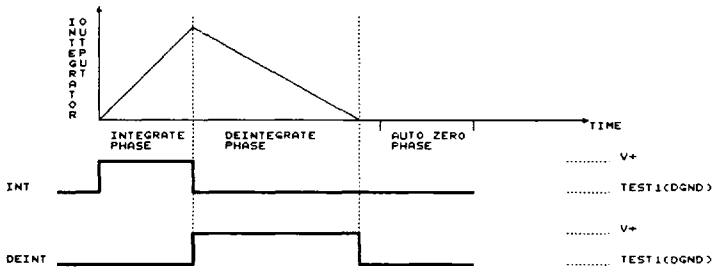


2. Serial Data Output



Timing Waveforms (continued)

3. INT, DEINT Output Waveform



Pin Descriptions

Pin No.		Designation	Description
UM7108A/B	UM7108F		
1	9	V+	Positive supply voltage
	7	INT	Integrate phase indicator. This pin is logic LOW normally but goes HIGH when integrate phase begins; goes LOW when integrate phase ends
	8	FREQ/$\overline{\text{VOLT}}$	Frequency counter/voltage measurement select pin. Connecting to V+ will enable the frequency counter, connecting to TEST1 or open will execute voltage measurement. This pin is internally pulled-down to TEST1
2	10	CONT/- /MHz	LCD segment drive for continuity, polarity and mega-Hz
3	11	B4/C4/DP3	LCD segment drive for "b" and "c" segments of MSD and decimal point 3
4	12	KHz/F3/E3	LCD segment drive for kilo-Hz and " f " and "e" segments of 3rd LSD
5	13	A3/G3/D3	LCD segment drive for "a" , "g" and "d" segments of 3rd LSD
6	14	B3/C3/DP2	LCD segment drive for "b" and "c" segments of 3rd LSD and decimal point 2
7	15	D-H/F2/E2	LCD segment drive for data-hold, " f " and "e" segments of 2nd LSD

Pin Descriptions (continued)

Pin No.		Designation	Description
UM7108A/B	UM7108F		
8	16	A2/G2/D2	LCD segment drive for "a", "g" and "d" segments of 2nd LSD
9	17	B2/C2/DP1	LCD segment drive for "b" and "c" segments of 2nd LSD and decimal point 1
10	18	P-H/F1/E1	LCD segment drive for peak-hold and " f " and "e" segments of LSD
11	19	A1/G1/D1	LCD segment drive for "a", "g" and "d" segments of LSD
12	20	B1/C1/BAT	LCD segment drive for "b" and "c" segments of LSD and low battery
13	21	COM1	LCD common driver #1
14	22	COM2	LCD common driver #2
15	23	COM3	LCD common driver #3
	24	FREQ - IN	Frequency counter input pin
16	25	DEINT	De-integrate phase indicator. This pin is logic LOW normally but goes HIGH when de-integrate phase begins; goes LOW when de-integrate phase ends
17	26	ANNUNC	Square wave output at the LCD backplane frequency, synchronized to COM1. Connecting an LCD segment to ANNUNC pin turns it on; connecting to backplane turns it off
18	27	DP1	1st decimal point select input for voltage measurement. This pin is internally pulled-down to TEST1
19	28	DP2	2nd decimal point select input for voltage measurement. This pin is internally pulled down to TEST1

Pin Descriptions (continued)

Pin No.		Designation	Description
UM7108A/B	UM7108F		
20	29	DP3	3rd decimal point select input for voltage measurement. This pin is internally pulled down to TEST1
21	30	RESET	Reset input pin. Connecting to V+ will cancel both Peak-hold and Data-hold functions. This pin is internally pulled-down to TEST1
22	31	PH – IP	Peak-hold input pin. Connecting to V+ will make the converter only update the readout if a new conversion value is greater than the preceding value. This pin is a toggle type input pin and is internally pulled-down to TEST1
23	32	DH – IP	Data-hold input pin. Connecting to V+ will make the converter hold the current readout and the converter operation. This pin is a toggle type input pin and is internally pulled-down to TEST1
	33	NC	No connection
24	34	BZOUT	Piezo buzzer output. 2.5 KHz audio frequency output can drive a piezo buzzer 1. Whenever the readout is less than 30 and BZINS is connected to V+ , BZOUT will generate a 2.5 KHz sound output. 2. Whenever the BZINM is connected to V+ it will force the BZOUT to generate a 2.5KHz sound audio output continuously
25 (UM7108A)	35	BZINS	Buzzer control slave input. This pin is internally pulled-down to TEST1. See BZOUT
	36	CLK	External clock input pin for serial data accessing, normally this clock signal is generated by external microcontroller
	37	SDO	Serial data output pin
25 (UM7108B)	38	BZINM	Buzzer control master pin. This pin is internally pulled-down to TEST1. See BZOUT

Pin Descriptions (continued)

Pin No.		Designation	Description
UM7108A/B	UM7108F		
	39	EOC	End of conversion indicator. When each conversion ends, this pin will generate a positive pulse. Normally, use this signal to interrupt microcontroller
26	40	V -	Negative power supply voltage. Connected to negative terminal of 9V battery
27	41	VINT	Integrator output. Connect to integration capacitor
28	42	VBUFF	Integration resistor connection. Use a 47KΩ resistor for 200.0 mV full-scale and a 470KΩ resistor for 2.000 V full-scale
29	43	CAZ	Autozero capacitor connection. Use a 0.47μF capacitor for 200.0 mV full-scale, and a 0.047μF capacitor for 2.000 V full-scale
30	44	VIN -	The analog low input signal is connected to this pin
31	45	VIN+	The analog high input signal is connected to this pin
32	46	ANA - COM	This pin is primarily used to set the analog ground reference for battery operation or in systems where the input signal is referenced to the power supply
33	47	CREF -	See pin 34
34	48	CREF+	A 0.1μF capacitor is used in most applications. If a large common-mode voltage exists and a 200 mV scale is used, a 1.0μF capacitor is recommended which will hold the rollover error to less than 0.5 count
35	1	VREF -	See pin 36

Pin Descriptions (continued)

Pin No.		Designation	Description
UM7108A/B	UM7108F		
36	2	V_{REF+}	This analog input is required to generate a full-scale output (1,999 counts). Place 100 mV between pin 35 and pin 36 for 200.0 mV full-scale. Place 1.00 V between pin 35 and pin 36 for 2.000 V full-scale
37	3	TEST1(DGND)	Lamp test. When connected to V+ all the segments will be turned on and readout should be 1888. It may also be used as an internal logical ground, nominally 4.7 V below the V+
38	4	OSC3	RC oscillator connection
39	5	OSC2	Crystal oscillator (input) connection
40	6	OSC1	Crystal oscillator (output) connection

Functional Description

An input signal to be measured is applied to the integrating capacitance for a fixed time as determined by a clock counter. The accumulated charge will be proportional to the input signal, for a fixed clock rate and constant current. The resulting integral is returned to zero by integrating a reference signal of polarity opposite that of the input signal. The length of time required for the integrator to return to zero, as measured with the clock counter to display at output, is proportional to the average magnitude of the input signal over the integration period.

A. Analog Section

Fig. 1 shows the block diagram of the Analog Section for UM7108.

Each measurement cycle is divided into three parts. These are : (1) Auto-zero [AZ]
(2) Signal integration [INT]
(3) Deintegration [DE]

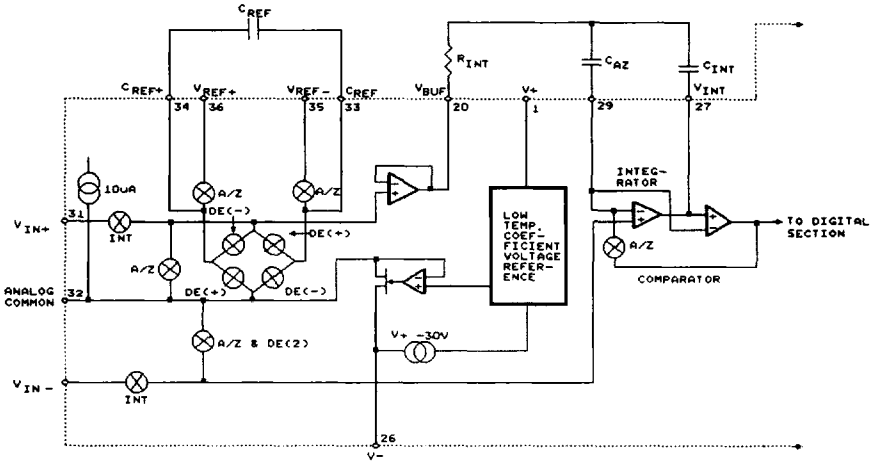


Figure 1. UM7108 Analog Section

1. Auto Zero Phase

During Auto-Zero, three things happen:

(1) V_{IN+} and V_{IN-} are disconnected from pin 30 and 31 and shorted to ANA-COM
(2) The reference capacitor is charged to the reference voltage.
(3) A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator and comparator.

2. Signal Integrate Phase

During signal integration, the auto-zero loop is opened, the internal short circuit is removed, and the internal inputs high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN-} and V_{IN+} for a fixed time (1000 counts). At the end of this phase, the polarity of the integrated signal is determined.

3. De-Integrate Phase

The final phase is de-integration, or reference integration. V_{IN-} is internally connected to ANA-COM and V_{IN+} is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required to return to zero is proportional to the input signal. Specifically, the digital reading displayed is $1000 \left(\frac{A_{IN}}{V_{REF}} \right)$.

4. Component Value Selection:

Integrating Resistor (R_{INT})

The buffer amplifier and integrator are designed with class A output stages with 100 μA of quiescent current each. They can supply 20 μA drive current with negligible linearity errors. R_{INT} should be large enough to remain in linear region but small enough to reduce the leakage current on the PC board. For 200.0mV full scale, R_{INT} is 47KΩ; at 2.000 Volt full scale a 470KΩ R_{INT} is needed.

Integrating Capacitor (CINT)

CINT should be chosen to give the maximum voltage swing without causing the saturation of integrator output swing. According to the superior temperature coefficient — 20ppm/ °C of analog common, analog common will be normally used as the differential voltage reference. It is fine for a nominal ±2.000V full scale integrator output swing. For 2 1/2 readings/ second (40 KHz clock), a 0.22μF capacitor is suggested. If a different oscillator frequency is used, CINT must be changed in inverse proportion to maintain the nominal ±2.000V full scale integrator output swing.
An additional requirement of RINT is that CINT must have low dielectric absorption to minimize rollover error. Polypropylene capacitors give undetectable errors at reasonable cost.

Reference Voltage Capacitor (CREF)

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on CREF. A 0.1μF capacitor gives good performance when VIN- is tied to analog common. If a large analog common voltage exists VREF- unequal analog common) and a 200.0mV scale is used, a larger value is required to prevent rollover error.
Generally 1.0μF will hold the rollover error to 0.5 count. In this case a mylar type dielectric capacitor is adequate.

Auto-Zero Capacitor (CAZ)

The CAZ value has some influence on system noise. The following combination is recommended:

Application	Adequate CAZ
200.0mV Full Scale	0.47μF
2.000V Full Scale	0.047μF

It is better to use a mylar type capacitor to implement CAZ.

Oscillator Components (Rosc, Cosc)

While using RC oscillator, the Rosc (between pin 39 and pin 40) should be 100KΩ and Cosc is selected from the following equation:

$$Fosc = \frac{0.45}{Rosc \times Cosc} \quad (Rosc \text{ in } M\Omega,\ Cosc \text{ in } \mu F)$$

Reference Voltage Selection

The analog input required to generate full scale output (2000 counts) is VIN = 2 VREF, thus:

Required Full Scale Voltage	VREF
200.0mV	100.0mV
2.000V	1.000V

However, in many applications where the A/D converter is connected to a transducer, there may exist a non-unity scale factor between the input voltage and the digital readout. For instance, a pressure transducer output is 400mV for 2000 lb/in^2, rather than dividing the input voltage by two, the VREF should be set to 200.0mV, then permit the transducer input to be used directly.
The differential voltage reference can also be used when a digital zero readout is required when VIN is not zero. This case is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and VIN and the transducer output is connected between VIN and analog common.

B. Digital Section

In the UM7108, the internal digital ground is generated from a 6.2 Volt Zener diode and a large p-channel follower. This supply is made stiff to absorb the relatively large capacitive current when the back plane (BP) is switched. The BP frequency is the clock frequency divided by 240. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible DC voltage exists across the segments.

1. System Timing

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phase. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes complete measure cycles of 4000 (16000 clock pulses) independent of input voltage. * As a matter of fact, the total measurement cycle is 4001 counts for measured values less than 2000 counts. The measurement cycle becomes 4000 counts for over-flow measurement.

2. Clock Circuit

UM7108A/B/F can use the following three clocking methods:

1. An external oscillator connected to OSC1 PIN.
2. A crystal between OSC2 PIN and OSC1 PIN.
3. An RC oscillator using all three pins (OSC3, OSC2 & OSC1).

To achieve maximum rejection of 50/60 Hz pick up, the signal integrate cycle should be a multiple of 50/60 Hz, the following table describes the selection of oscillator frequencies for 50 or 60 Hz respectively.

	Oscillator Frequencies
50 Hz	*..40 KHz, 50 KHz, 66 2/3 KHz, 100 KHz...
60 Hz	*..33 1/3 KHz, 40 KHz, 48 KHz, 60 KHz, 80 KHz, 100 KHz....

*Note that 40 KHz (2.5 readings/second) will reject both 50 and 60 Hz line noise.

3. LCD Display

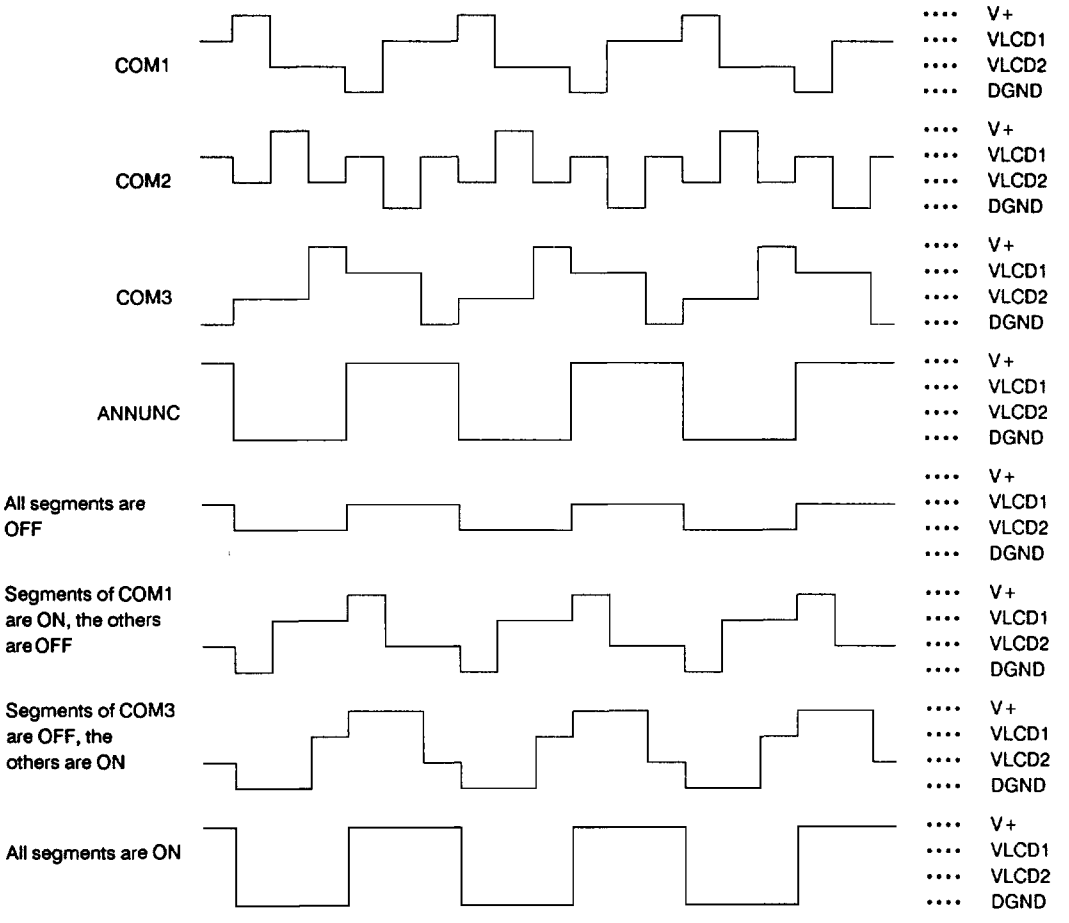
The UM7108A/B/F drives a triplex LCD with three commons. This LCD includes 3 1/2-digits, three decimal point polarity sign and annunciators for peakhold, data-hold, continuity, frequency and low battery. The following figure indicates the assignments of the display segments to the common and segment drive lines.

UM7108A/B Pin No.	UM7108F Pin No.	COM1	COM2	COM3
2	10	CONT	-	MHz
3	11	B4	C4	DP3
4	12	KHz	F3	E3
5	13	A3	G3	D3
6	14	B3	C3	DP2
7	15	D - H	F2	E2
8	16	A2	G2	D2
9	17	B2	C2	DP1
10	18	P - H	F1	E1
11	19	A1	G1	D1
12	20	B1	C1	BAT
13	21	COM1	-	-
14	22	-	COM2	-
15	23	-	-	COM3

The LCD common drive frequency is obtained by dividing the oscillator frequency (Fclock) by 240.

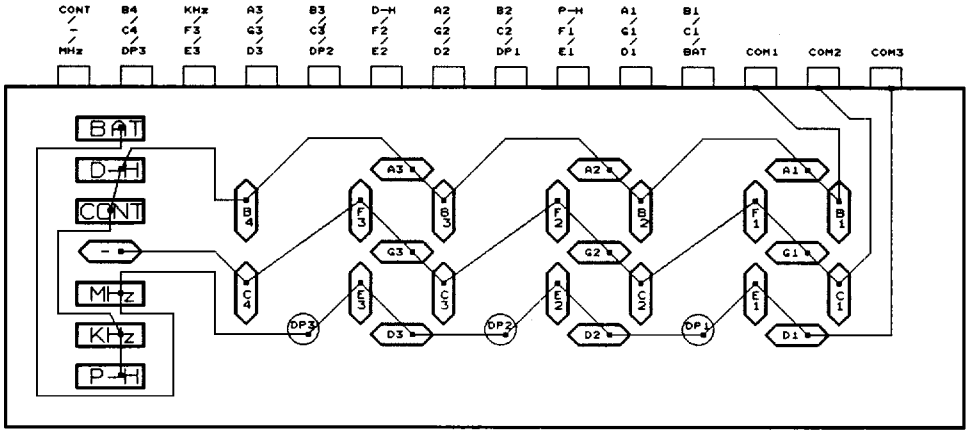
$$Flcd = \frac{Fclock}{240}$$

The LCD waveform is as follows :

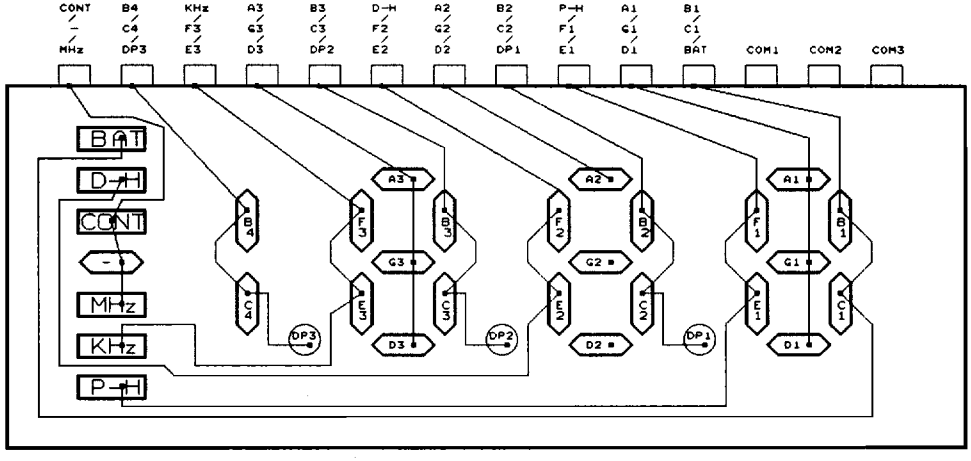


The annunciator output is a square wave running at the LCD backplane frequency (ex. 167 Hz for Fclock = 40 KHz). The pk-pk amplitude is equal to (V+ - DGND). Connecting an annunciator of the LCD to the ANNUNC pin turns the annunciator on; connecting it to its common turns it off.

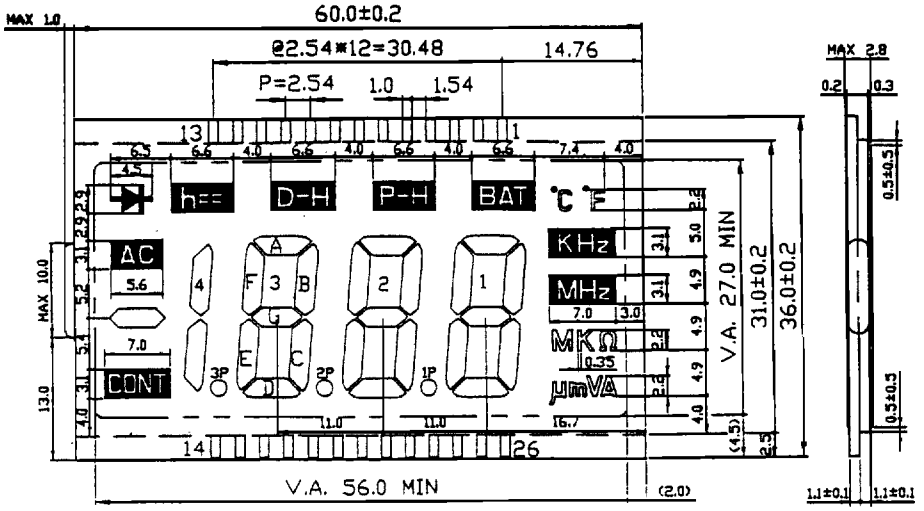
UM7108A/B/F LCD COMMON LAYOUT

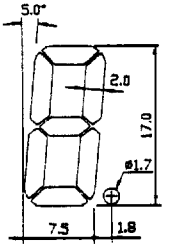


UM7108A/B/F LCD SEGMENT LAYOUT



UMC also provides the following LCD sample for UM7108A/B/F to achieve full features





Viewing Direction

Notes:	1. Display Type	Twisted Nematic Display
	2. Viewing Direction	6 O'Clock
	3. Polarizer Mode	Reflective/Positive
	4. Drive Method	1/3 Duty 1/3 Bias
	5. Operating Voltage	5.0V
	6. Operating Temp	-10°C ~ +60°C
	7. Storage Temp	-20°C ~ +70°C
	8. Connector	Zebra

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13
COM3	COM3	/	/	BAT	1D	1E	1P	2D	2E	2P	3D	3E	3P
COM2	/	COM2	/	1C	1G	1F	2C	2G	2F	3C	3G	3F	4C
COM1	/	/	COM1	1B	1A	P-H	2B	2A	D-H	3B	3A	KHz	4B

PIN	14	15	16	17	18	19	20	21	22	23	24	25	26
COM3	/	/	/	MHz	/	/	/	/	/	/	/	/	/
COM2	/	/	/		/	/	/	/	/	/	/	/	/
COM1	hFE		AC	CONT	M	K	Ω	μ	m	V	A	°C	°F

4. Frequency Counter

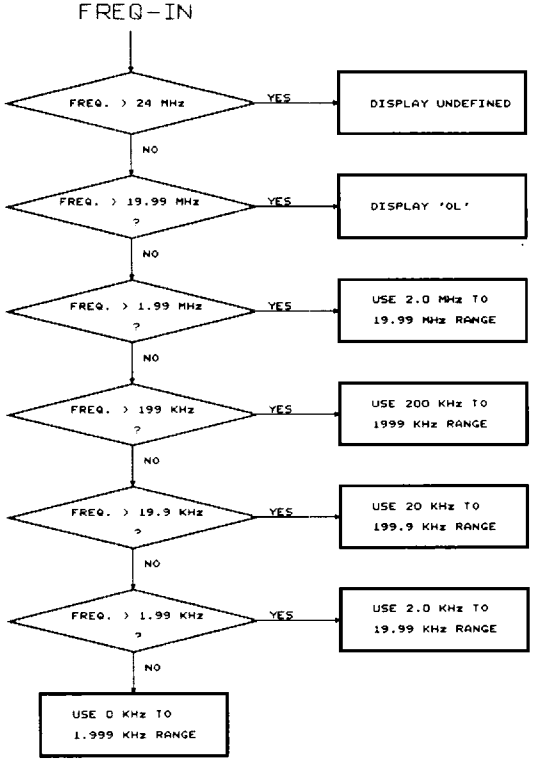
In addition to serving as an analog-to-digital converter, the UM7108F also provides 2 KHz to 20 MHz five decade auto-range frequency counter. In the counter mode, pulses at the FREQ-IN will be counted and displayed.

The UM7108F frequency counter derives its time base from the clock oscillator and gets one readout per second. The frequency counter accuracy is determined by the oscillator accuracy. For accurate frequency measurement, a 40 KHz quartz crystal oscillator is recommended.

The decimal points are automatically set in frequency mode, the following table indicates the auto-range decimal points and annunciator selection versus frequency counter input (Fin).

FREQ-IN	Decimal Point	Annunciator
0 KHz to 1.999 KHz	DP3	KHz
2.0 KHz to 19.99 KHz	DP2	KHz
20 KHz to 199.9 KHz	DP1	KHz
200 KHz to 1999 KHz	NONE	KHz
2.0 MHz to 19.99 MHz	DP2	MHz

Auto-Range Frequency Counter Range Selection Algorithm

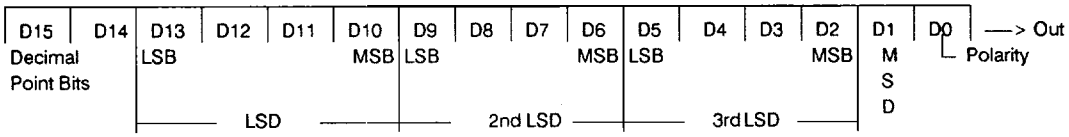


5. Serial Data Output

In addition to the LCD output, the UM7108F provides serial data output for use in connection with micro-controllers. During this operation, UM7108F uses CLK, SDO and EOC pins. The following is the timing description of this connection.

The EOC pin will rise HIGH at the end of conversion and the content of serial output data buffer will update simultaneously.
The waveform of EOC pin will go LOW as soon as CLK pin receives clock signal. Otherwise the EOC pin will stay HIGH and then go LOW in 10 ms.

Serial Data Output Format



1. Voltage Mode:

D0 (Polarity) — '1' —> Plus; '0' —> Minus

D1 (MSD) — '1' —> MSD = 1; '0' —> MSD = 0

D2 to D5 for 3rd LSD (From 0000 TO 1001)
D6 to D9 for 2nd LSD (From 0000 TO 1001)
D10 to D13 for LSD (From 0000 TO 1001)

D14 & D15 for Decimal Point Bits

D14	D15	Decimal Point
0	0	None
0	1	DP1
1	0	DP2
1	1	DP3

2. Frequency Mode:

D0 (KHz/MHz) — '1' —> MHz; '0' —> KHz

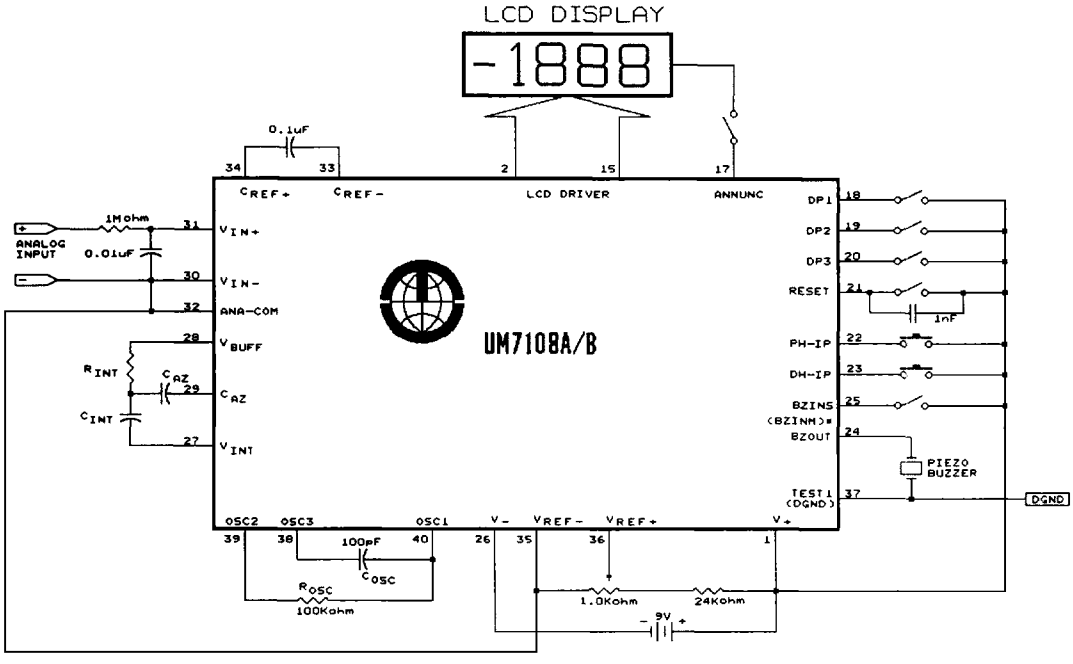
The rest are same as voltage mode.

Special Data Format

Items	D15 . . . . . D6	D5	D4	D3	D2	D1	D0
(1) Initial State (0000)	Random and don't care	1	1	1	1	1	1
(2) Positive Overflow (OL)		0	0	1	1	1	1
(3) Negative Overflow (- OL)		0	0	1	1	1	0

Application Circuits (for reference only)

(1) For UM7108A/B

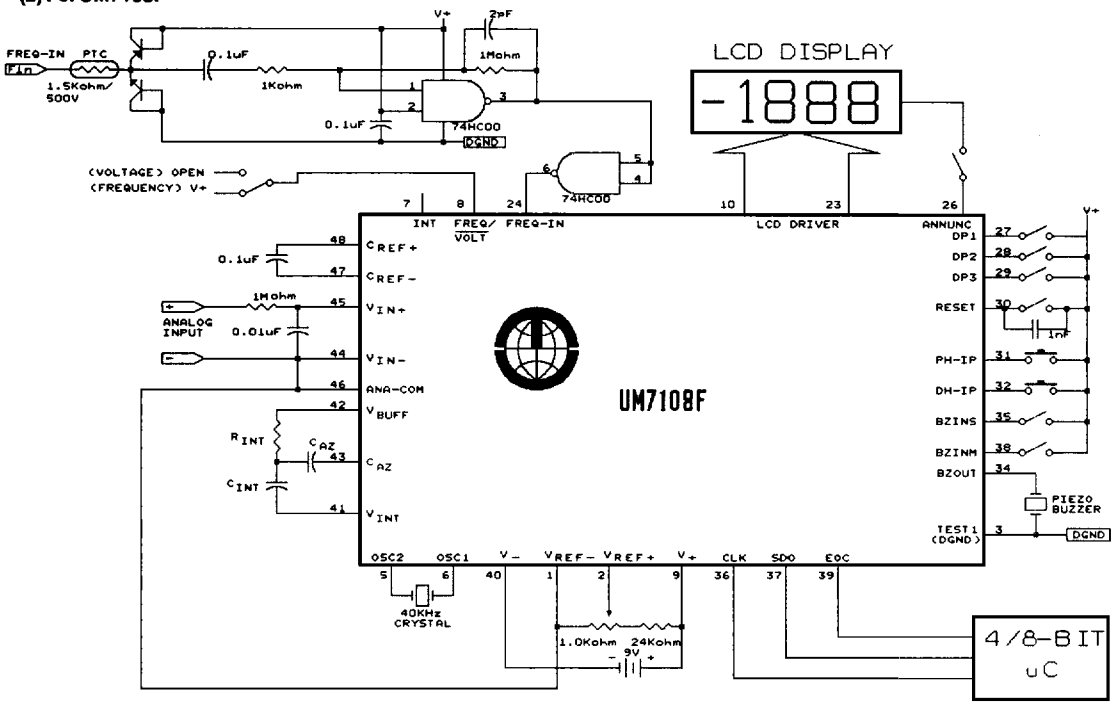


Note: Pin 25 [BZINS— UM7108A
BZINM— UM7108B

Component Value	Nominal Full-Scale Voltage	
	2.000V	200.0mV
CAZ	0.047μF	0.47μF
RINT	470KΩ	47KΩ
CINT	0.22μF	0.22μF
VREF	1.000V	100.0mV

Application Circuits (continued)

(2) For UM7108F



Component Value	Nominal Full-Scale Voltage	
	2.000V	200.0mV
C_{AZ}	0.047μF	0.47μF
R_{INT}	470KΩ	47KΩ
C_{INT}	0.22μF	0.22μF
V_{REF}	1.000V	100.0mV

Ordering Information

Part No.	Buzzer Input Selection	Package
UM7108A	BZINS	40L DIP
UM7108B	BZINM	40L DIP
UM7108F	BZINS, BZINM	48L QFP