

SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

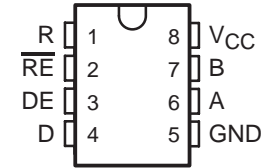
SLLS067G – AUGUST 1990 – REVISED APRIL 2006

- Bidirectional Transceiver
- Meets or Exceeds the Requirements of ANSI Standard TIA/EIA-485-A and ISO 8482:1987(E)
- High-Speed Low-Power LinBiCMOS™ Circuitry
- Designed for High-Speed Operation in Both Serial and Parallel Applications
- Low Skew
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Very Low Disabled Supply Current . . . 200 μ A Maximum
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Thermal-Shutdown Protection
- Driver Positive-and Negative-Current Limiting
- Open-Circuit Failsafe Receiver Design
- Receiver Input Sensitivity . . . ± 200 mV Max
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

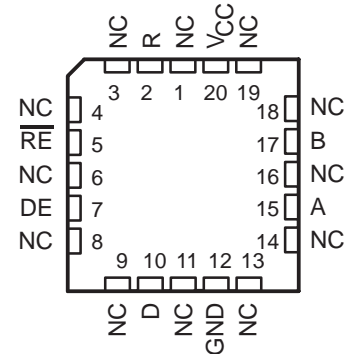
description

The SN55LBC176, SN65LBC176, SN65LBC176Q, and SN75LBC176 differential bus transceivers are monolithic, integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and meet ANSI Standard TIA/EIA-485-A (RS-485) and ISO 8482:1987(E).

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_{IA} - V_{IB}$	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS and LinASIC are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000–2006, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

SLLS067G – AUGUST 1990 – REVISED APRIL 2006

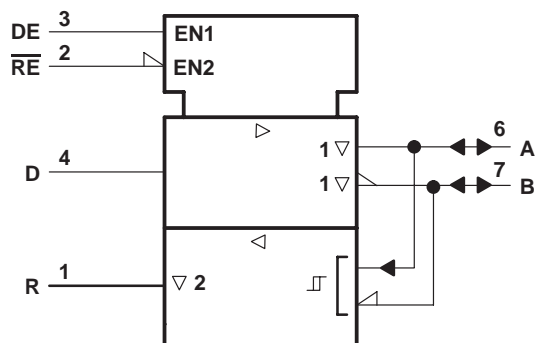
description (continued)

The SN55LBC176, SN65LBC176, SN65LBC176Q, and SN75LBC176 combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Very low device supply current can be achieved by disabling the driver and the receiver.

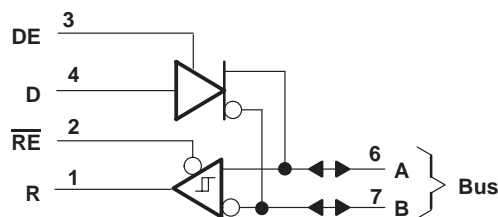
These transceivers are suitable for ANSI Standard TIA/EIA-485 (RS-485) and ISO 8482 applications to the extent that they are specified in the operating conditions and characteristics section of this data sheet. Certain limits contained in TIA/EIA-485-A and ISO 8482:1987 (E) are not met or cannot be tested over the entire military temperature range.

The SN55LBC176 is characterized for operation from -55°C to 125°C . The SN65LBC176 is characterized for operation from -40°C to 85°C , and the SN65LBC176Q is characterized for operation from -40°C to 125°C . The SN75LBC176 is characterized for operation from 0°C to 70°C .

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

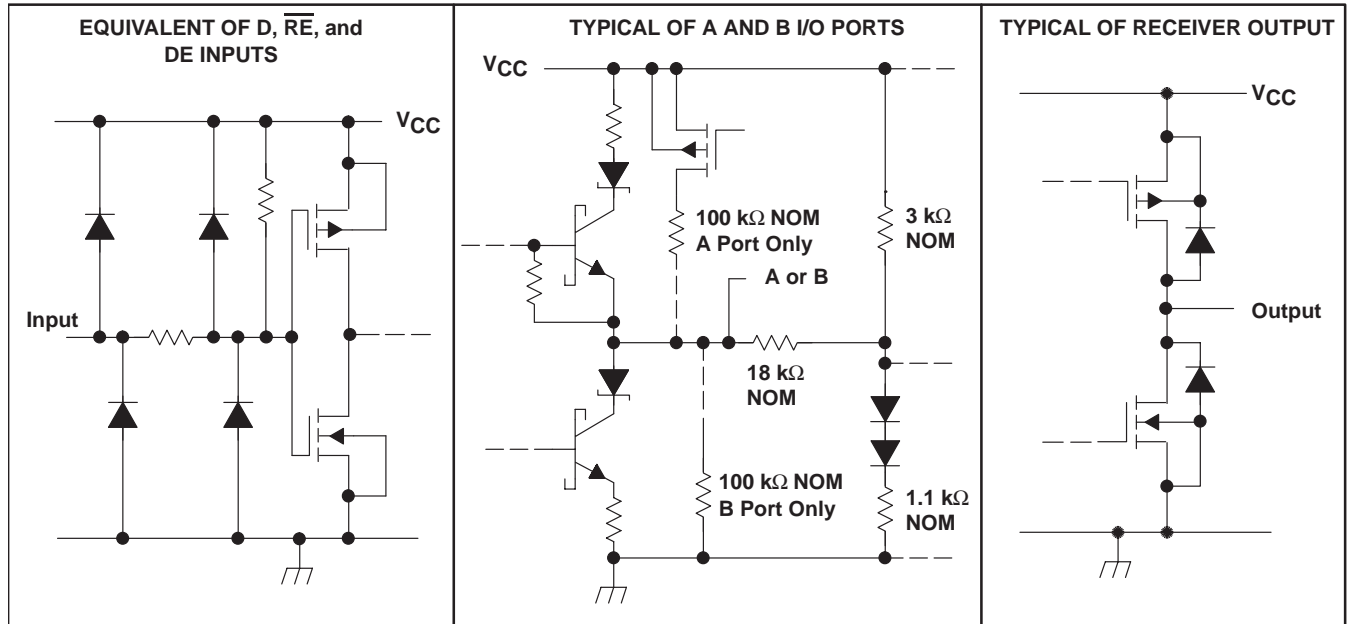
AVAILABLE OPTIONS

T_A	PACKAGE	PART NUMBER	PART MARKING
0°C to 70°C	SOP	SN75LBC176D	7LB176
	PDIP	SN75LBC176P	75LBC176
-40°C to 85°C	SOP	SN65LBC176D	6LB176
	PDIP	SN65LBC176P	65LBC176
-40°C to 110°C	SOP	SN65LBC176QD	LB176Q
	SOP	SN65LBC176QDR	LB176Q
-55°C to 125°C	LCCC	SNJ55LBC176FK	SNJ55LBC176FK
	CDIP	SNJ55LBC176JG	SNJ55LBC176

SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

SLLS067G – AUGUST 1990 – REVISED APRIL 2006

schematics of inputs and outputs



absolute maximum ratings†

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	-10 V to 15 V
Input voltage, V_I (D, DE, R, or \overline{RE})	-0.3 V to $V_{CC} + 0.5$ V
Receiver output current, I_O	± 10 mA
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	THERMAL MODEL	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 110^\circ\text{C}$ POWER RATING
D	Low K^\dagger	526 mW	5.0 mW/°C	301 mW	226 mW	—
	High K^\ddagger	882 mW	8.4 mW/°C	504 mW	378 mW	—
P		840 mW	8.0 mW/°C	480 mW	360 mW	—
JG		1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
FK		1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW

† In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51-3.

‡ In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51-7.



SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

SLLS067G – AUGUST 1990 – REVISED APRIL 2006

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		-7		12	V
High-level input voltage, V_{IH}	D, DE, and \overline{RE}	2			V
Low-level input voltage, V_{IL}	D, DE, and \overline{RE}			0.8	V
Differential input voltage, V_{ID} (see Note 2)		-12		12	V
High-level output current, I_{OH}	Driver	-60			mA
	Receiver	-400			μ A
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Junction temperature, T_J				140	$^{\circ}$ C
Operating free-air temperature, T_A	SN55LBC176	-55		125	$^{\circ}$ C
	SN65LBC176	-40		85	
	SN65LBC176Q	-40		125	
	SN75LBC176	0		70	

NOTE 2: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

SLLS067G – AUGUST 1990 – REVISED APRIL 2006

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT	
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$		-1.5		V	
V_O	Output voltage	$I_O = 0$		0	6	V	
$ V_{OD1} $	Differential output voltage	$I_O = 0$		1.5	6	V	
$ V_{OD2} $	Differential output voltage	$R_L = 54 \Omega$, See Note 3	See Figure 1,	55LBC176, 65LBC176, 65LBC176Q	1.1	V	
				75LBC176	1.5		5
V_{OD3}	Differential output voltage	$V_{\text{test}} = -7 \text{ V to } 12 \text{ V}$, See Note 3	See Figure 2,	55LBC176, 65LBC176, 65LBC176Q	1.1	V	
				75LBC176	1.5		5
$\Delta V_{OD} $	Change in magnitude of differential output voltage [†]	$R_L = 54 \Omega$ or 100Ω , See Figure 1		-0.2	0.2	V	
V_{OC}	Common-mode output voltage			-1	3	V	
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage [†]			-0.2	0.2	V	
I_O	Output current	Output disabled, See Note 4	$V_O = 12 \text{ V}$	1		mA	
			$V_O = -7 \text{ V}$	-0.8			
I_{IH}	High-level input current	$V_I = 2.4 \text{ V}$		-100		μA	
I_{IL}	Low-level input current	$V_I = 0.4 \text{ V}$		-100		μA	
I_{OS}	Short-circuit output current	$V_O = -7 \text{ V}$		-250		mA	
		$V_O = 0$		-150			
		$V_O = V_{CC}$		250			
		$V_O = 12 \text{ V}$					
I_{CC}	Supply current	$V_I = 0$ or V_{CC} , No load	Receiver disabled and driver enabled	55LBC176, 65LBC176Q	1.75		mA
				65LBC176, 75LBC176	1.5		
			Receiver and driver disabled	55LBC176, 65LBC176Q	0.25		
				65LBC176, 75LBC176	0.2		

[†] $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input changes from a high level to a low level.

- NOTES: 3. This device meets the V_{OD} requirements of TIA/EIA-485-A above 0°C only.
4. This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions.



SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

SLLS067G – AUGUST 1990 – REVISED APRIL 2006

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	SN55LBC176 SN65LBC176Q			SN65LBC176 SN75LBC176			UNIT
		MIN	TYP	MAX	MIN	TYP†	MAX	
$t_{d(OD)}$ Differential output delay time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3	8		31	8		25	ns
$t_t(OD)$ Differential output transition time			12			12		ns
$t_{sk(p)}$ Pulse skew ($ t_{d(ODH)} - t_{d(ODL)} $)				6		0	6	ns
t_{PZH} Output enable time to high level	$R_L = 110 \Omega$, See Figure 4			65			35	ns
t_{PZL} Output enable time to low level	$R_L = 110 \Omega$, See Figure 5			65			35	ns
t_{PHZ} Output disable time from high level	$R_L = 110 \Omega$, See Figure 4			105			60	ns
t_{PLZ} Output disable time from low level	$R_L = 110 \Omega$, See Figure 5			105			35	ns

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-485
V_O	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_o
$ V_{OD2} $	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $	V_t (test termination measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{Os} $
$\Delta V_{OC} $	$ V_{Os} - \bar{V}_{Os} $
I_{OS}	None
I_O	I_{ia}, I_{ib}



SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

SLLS067G – AUGUST 1990 – REVISED APRIL 2006

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7\text{ V}$,	$I_O = -0.4\text{ mA}$			0.2	V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5\text{ V}$,	$I_O = 8\text{ mA}$			-0.2‡	V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$) (see Figure 4)				50		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18\text{ mA}$		-1.5			V
V_{OH}	High-level output voltage	$V_{ID} = 200\text{ mV}$, See Figure 6	$I_{OH} = -400\text{ }\mu\text{A}$,	2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = -200\text{ mV}$, See Figure 6	$I_{OL} = 8\text{ mA}$,			0.45	V
I_{OZ}	High-impedance-state output current	$V_O = 0.4\text{ V to }2.4\text{ V}$		-20		20	μA
I_I	Line input current	Other input = 0 V, See Note 5	$V_I = 12\text{ V}$			1	mA
			$V_I = -7\text{ V}$	-0.8			
I_{IH}	High-level enable-input current	$V_{IH} = 2.7\text{ V}$		-100			μA
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4\text{ V}$		-100			μA
r_I	Input resistance			12			k Ω
I_{CC}	Supply current	$V_I = 0\text{ or }V_{CC}$, No load	Receiver enabled and driver disabled			3.9	mA
			Receiver and driver disabled	SN55LBC176, SN65LBC176, SN65LBC176Q		0.25	
				SN75LBC176		0.2	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.

NOTE 5: This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 15\text{ pF}$

PARAMETER	TEST CONDITIONS	SN55LBC176 SN65LBC176Q		SN65LBC176 SN75LBC176		UNIT	
		MIN	MAX	MIN	TYP†		MAX
t_{PLH}	Propagation delay time, low- to high-level single-ended output	11	37	11		33	ns
t_{PHL}	Propagation delay time, high- to low-level single-ended output	11	37	11		33	ns
$t_{sk(p)}$	Pulse skew ($ t_{PLH} - t_{PHL} $)		10		3	6	ns
t_{PZH}	Output enable time to high level		35			35	ns
t_{PZL}	Output enable time to low level		35			30	ns
t_{PHZ}	Output disable time from high level		35			35	ns
t_{PLZ}	Output disable time from low level		35			30	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.



SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

SLLS067G – AUGUST 1990 – REVISED APRIL 2006

PARAMETER MEASUREMENT INFORMATION

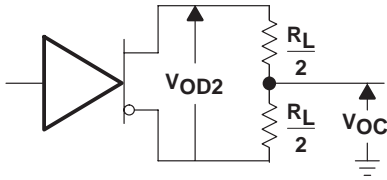


Figure 1. Driver V_{OD} and V_{OC}

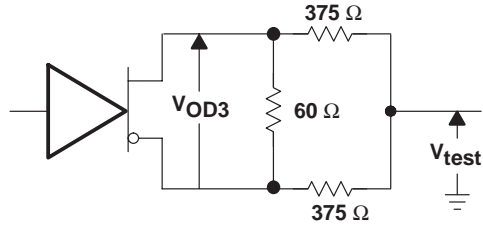
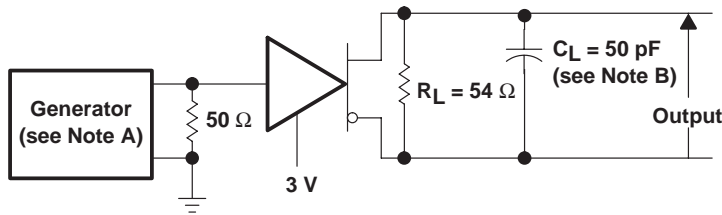
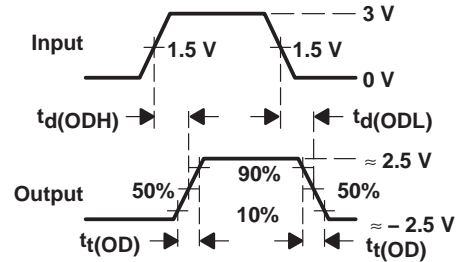


Figure 2. Driver V_{OD3}

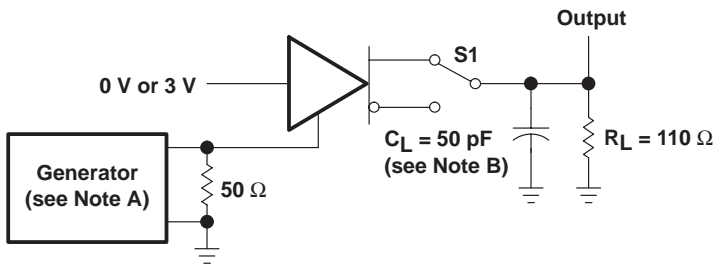


TEST CIRCUIT

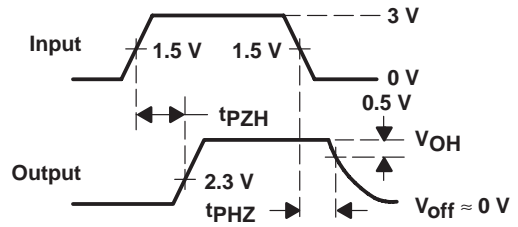


VOLTAGE WAVEFORMS

Figure 3. Driver Test Circuit and Voltage Waveforms

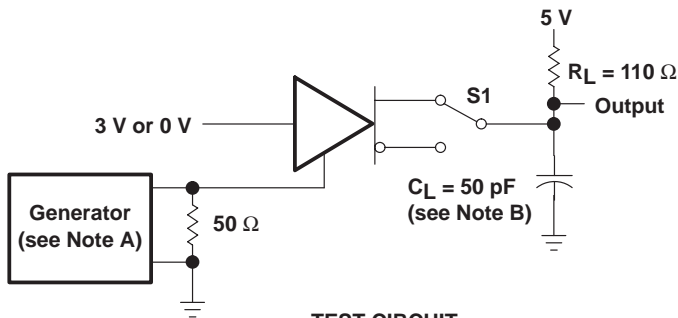


TEST CIRCUIT

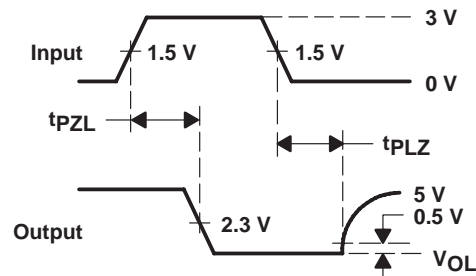


VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

SLLS067G – AUGUST 1990 – REVISED APRIL 2006

PARAMETER MEASUREMENT INFORMATION

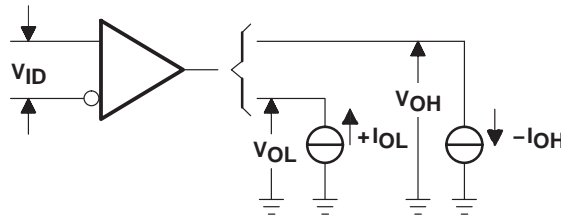
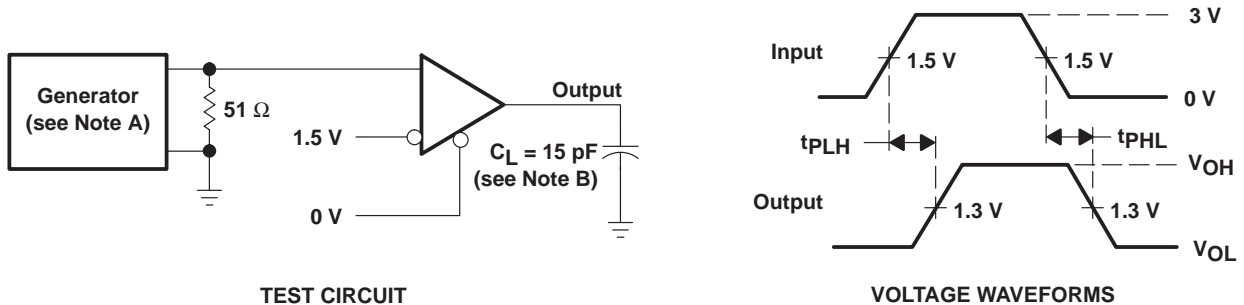


Figure 6. Receiver V_{OH} and V_{OL}



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

THERMAL CHARACTERISTICS – D PACKAGE

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Junction-to-ambient thermal resistance, θ_{JA} [†]	Low-K board, no air flow		199.4		°C/W
	High-K board, no air flow		119		
Junction-to-board thermal resistance, θ_{JB}	High-K board, no air flow		67		
Junction-to-case thermal resistance, θ_{JC}			46.6		
Average power dissipation, $P_{(AVG)}$	$R_L = 54 \Omega$, input to D is 10 Mbps 50% duty cycle square wave, $V_{CC} = 5.25$ V, $T_J = 130$ °C.			330	mW
Thermal shutdown junction temperature, T_{SD}			165		°C

[†] See TI application note literature number SZZA003, Package Thermal Characterization Methodologies, for an explanation of this parameter.

SN55LBC176, SN65LBC176, SN65LBC176Q, SN75LBC176 DIFFERENTIAL BUS TRANSCEIVERS

SLLS067G – AUGUST 1990 – REVISED APRIL 2006

PARAMETER MEASUREMENT INFORMATION

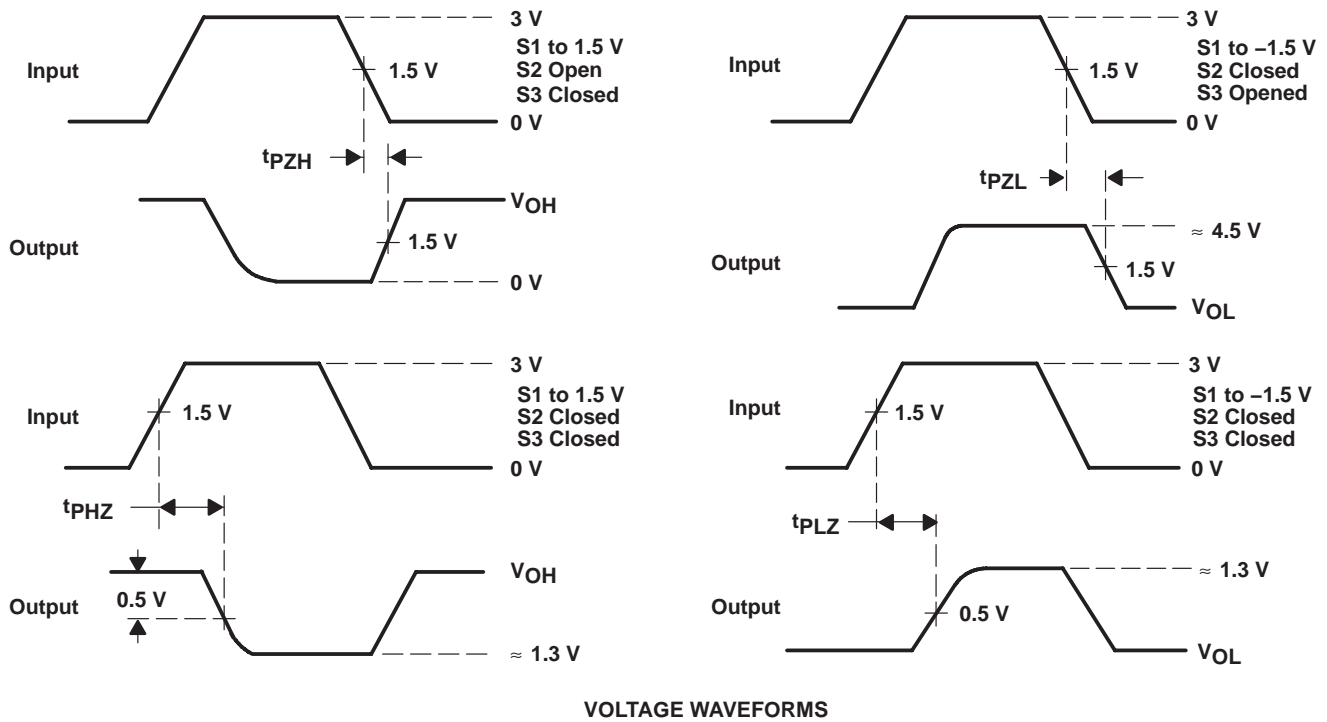
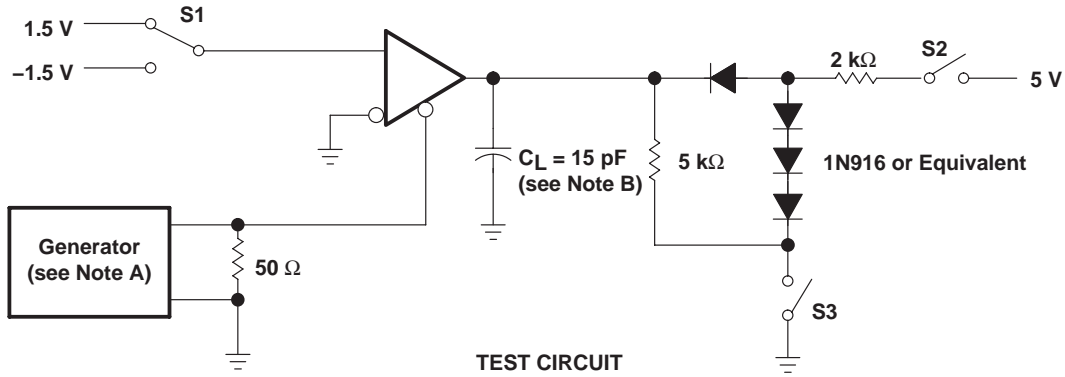


Figure 8. Receiver Test Circuit and Voltage Waveforms

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

THERMAL CHARACTERISTICS OF IC PACKAGES

Θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

Θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

Θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. Θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in Θ_{JA} can be measured between these two test cards

Θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

Θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with Θ_{JB} in 1-dimensional thermal simulation of a package system.

Θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. Θ_{JB} is only defined for the high-k test card.

Θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 1).

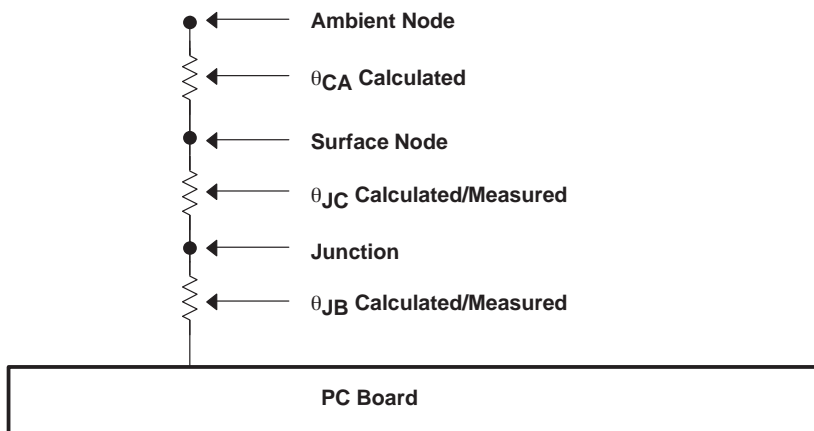


Figure 1. Thermal Resistance

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9318301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9318301QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
SN65LBC176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC176DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC176DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC176P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC176PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC176QD	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LBC176QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC176QDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65LBC176QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC176DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC176DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC176P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC176PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ55LBC176FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ55LBC176JG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS

compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55LBC176, SN65LBC176, SN75LBC176 :

- Automotive: [SN65LBC176-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75LBC176DR	SOIC	D	8	2500	340.5	338.1	20.6

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



4040107/C 08/96

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

P (R-PDIP-T8)

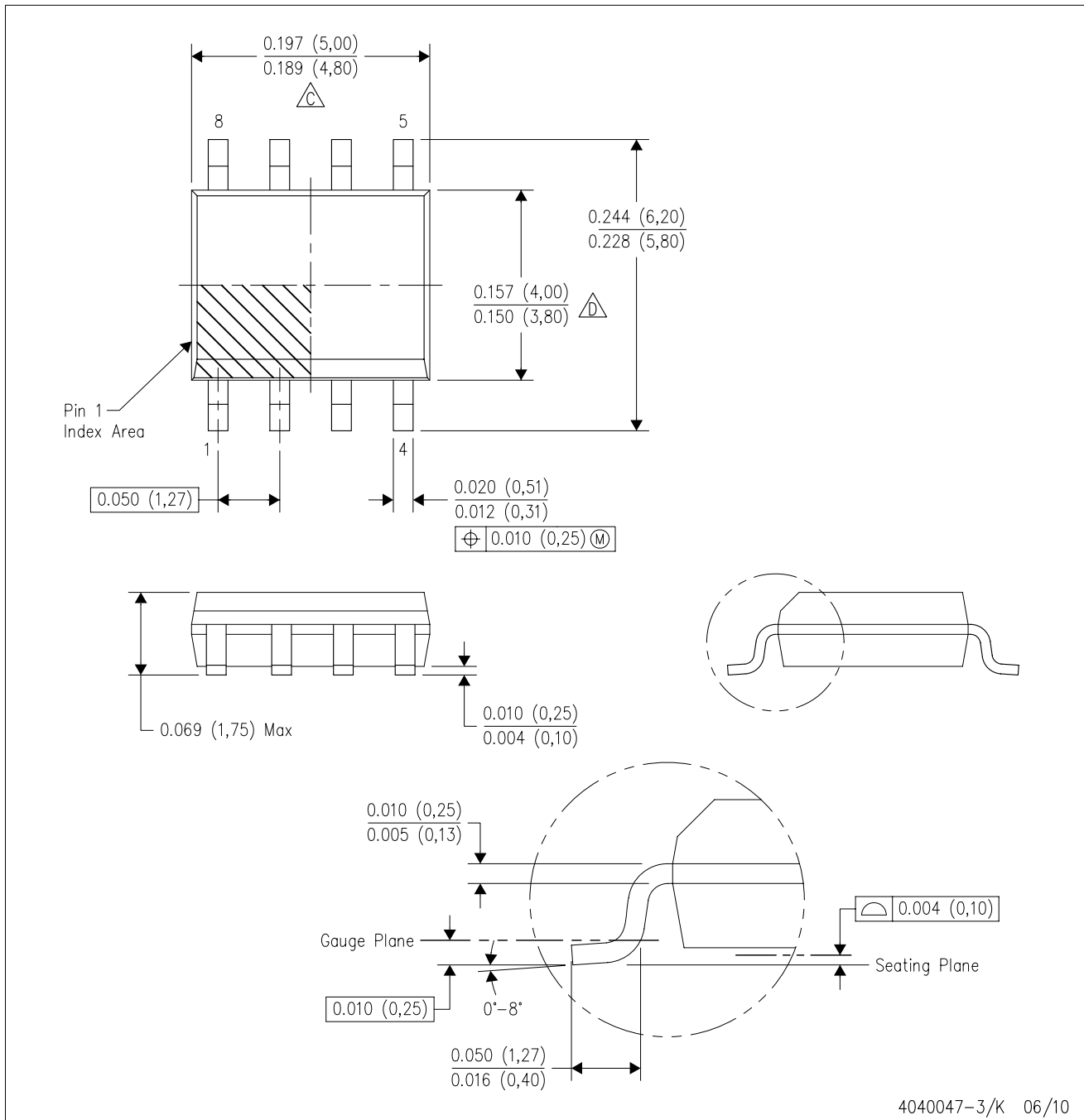
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

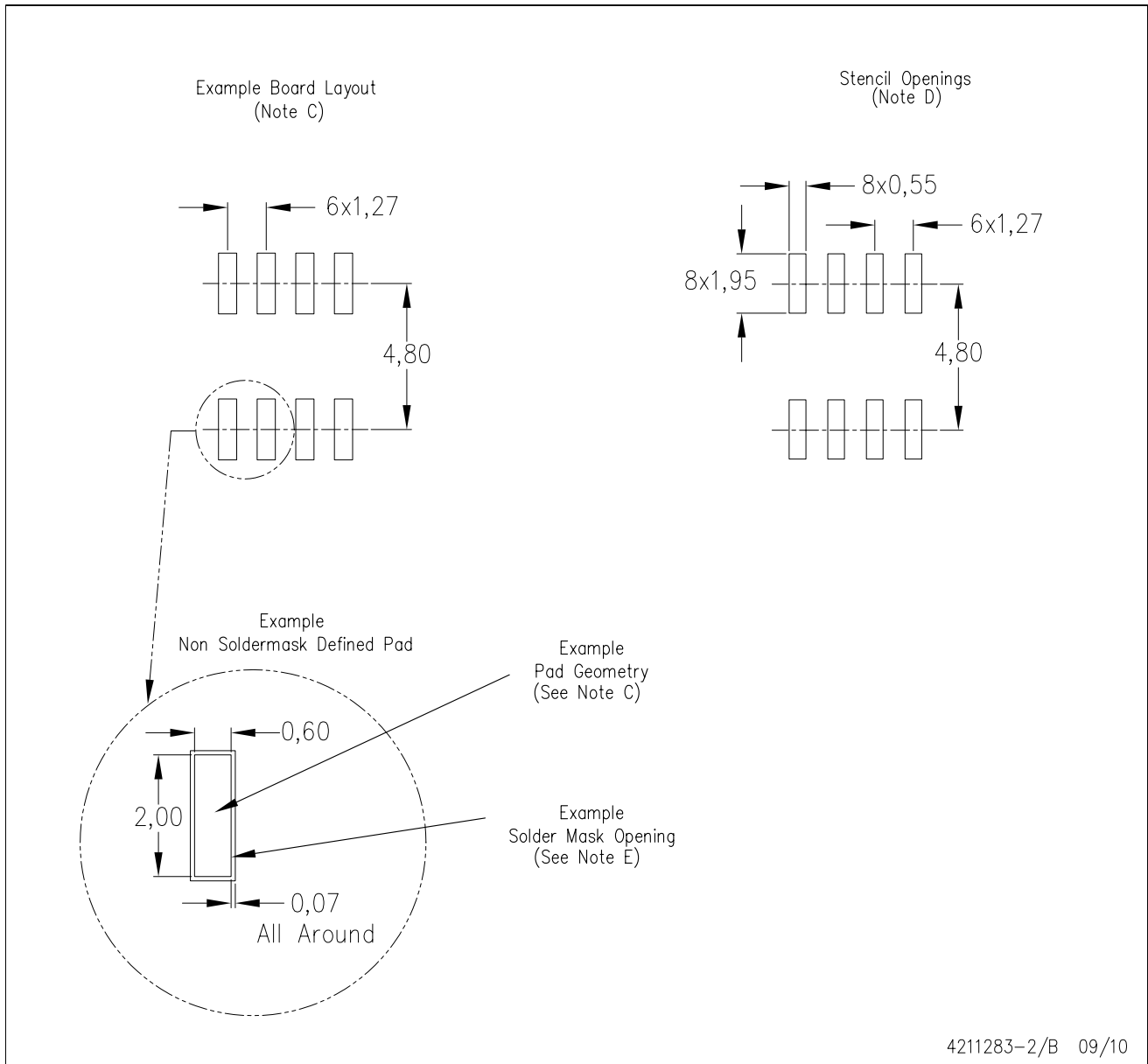
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps