

CURRENT-LIMITED, POWER-DISTRIBUTION SWITCHES

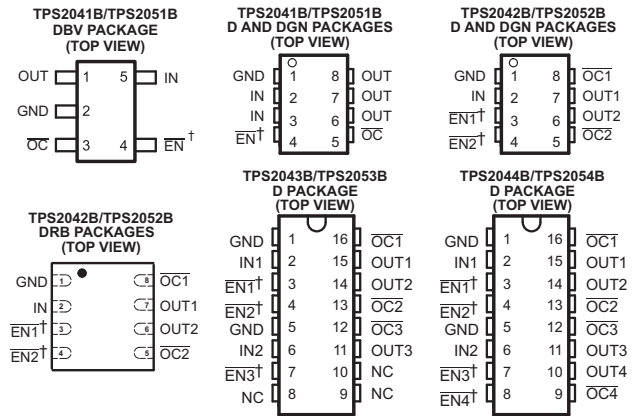
Check for Samples: [TPS2041B](#), [TPS2042B](#), [TPS2043B](#), [TPS2044B](#), [TPS2051B](#), [TPS2052B](#), [TPS2053B](#), [TPS2054B](#)

FEATURES

- 70-mΩ High-Side MOSFET
- 500-mA Continuous Current
- Thermal and Short-Circuit Protection
- Accurate Current Limit (0.75 A min, 1.25 A max)
- Operating Range: 2.7 V to 5.5 V
- 0.6-ms Typical Rise Time
- Undervoltage Lockout
- Deglitched Fault Report (\overline{OC})
- No \overline{OC} Glitch During Power Up
- Maximum Standby Supply Current: 1- μ A (Single, Dual) or 2- μ A (Triple, Quad)
- Ambient Temperature Range: -40°C to 85°C
- UL Recognized, File Number E169910
- Additional UL Recognition for TPS2042B and TPS2052B for Ganged Configuration

APPLICATIONS

- Heavy Capacitive Loads
- Short-Circuit Protections



† All enable inputs are active high for the TPS205xB series.
 NC - No connect

DESCRIPTION

The TPS204xB/TPS205xB power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices incorporate 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (\overline{OCx}) logic output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1 A typically.

| GENERAL SWITCH CATALOG | | | | | | |
|---|---|---|--|--|---|--|
| <p>33 mΩ, Single</p> <p>TPS201xA 0.2 A to 2 A TPS202x 0.2 A to 2 A TPS203x 0.2 A to 2 A</p> | <p>80 mΩ, Single</p> <p>TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A</p> | <p>80 mΩ, Dual</p> <p>TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A</p> | <p>80 mΩ, Dual</p> <p>TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA</p> | <p>80 mΩ, Triple</p> <p>TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A</p> | <p>80 mΩ, Quad</p> <p>TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA</p> | <p>80 mΩ, Quad</p> <p>TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA</p> |



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTION AND ORDERING INFORMATION

| T _A | ENABLE | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT | TYPICAL SHORT- CIRCUIT CURRENT LIMIT AT 25°C | NUMBER OF SWITCHES | PACKAGED DEVICES ^{(1) (2)} | | | |
|------------------|-------------|--|---|--------------------------|-------------------------------------|-----------|--------------|-------------|
| | | | | | MSOP (DGN) | SOIC (D) | SOT-23 (DBV) | SON (DRB) |
| -40°C to 85°C | Active low | 0.5 A | 1 A | Single | TPS2041BDGN | TPS2041BD | TPS2041BDBV | |
| | Active high | | | Single | TPS2051BDGN | TPS2051BD | TPS2051BDBV | |
| | Active low | | | Dual | TPS2042BDGN | TPS2042BD | | TPS2042BDRB |
| | Active high | | | Dual | TPS2052BDGN | TPS2052BD | | TPS2052BDRB |
| | Active low | | | Triple | -- | TPS2043BD | | |
| | Active high | | | Triple | -- | TPS2053BD | | |
| | Active low | | | Quad | -- | TPS2044BD | | |
| | Active high | | | Quad | -- | TPS2054BD | | |

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., TPS2042BDR).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | UNIT | |
|--|-------------------------------|-------|
| Input voltage range, V _{I(IN)} , V _{I(INx)} ⁽²⁾ | -0.3 V to 6 V | |
| Output voltage range, V _{O(OUT)} , V _{O(OUTx)} ⁽²⁾ | -0.3 V to 6 V | |
| Input voltage range, V _{I(EN)} , V _{I(ENx)} , V _{I(EN)} , V _{I(ENx)} | -0.3 V to 6 V | |
| Voltage range, V _{I(OC)} , V _{I(OCC)} | -0.3 V to 6 V | |
| Continuous output current, I _{O(OUT)} , I _{O(OUTx)} | Internally limited | |
| Continuous total power dissipation | See Dissipation Rating Table | |
| Operating virtual junction temperature range, T _J | -40°C to 125°C | |
| Storage temperature range, T _{stg} | -65°C to 150°C | |
| Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds | 260°C | |
| Electrostatic discharge (ESD) protection | Human body model MIL-STD-883C | 2 kV |
| | Charge device model (CDM) | 500 V |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND.

DISSIPATING RATING TABLE

| PACKAGE | THERMAL RESISTANCE, θ _{JA} | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|-------------------------------|--|---------------------------------------|--|---------------------------------------|---------------------------------------|
| DGN-8 | | 1712.3 mW | 17.123 mW/°C | 941.78 mW | 684.93 mW |
| D-8 | | 585.82 mW | 5.8582 mW/°C | 322.20 mW | 234.32 mW |
| D-16 | | 898.47 mW | 8.9847 mW/°C | 494.15 mW | 359.38 mW |
| DBV-5 | | 285 mW | 2.85 mW/°C | 155 mW | 114 mW |
| DRB-8 (Low-K) ⁽¹⁾ | 270 °C/W | 370 mW | 3.71 mW/°C | 203 mW | 148 mW |
| DRB-8 (High-K) ⁽²⁾ | 60 °C/W | 1600 mW | 16.67 mW/°C | 916 mW | 866 mW |

(1) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad. See TI application note [SLMA002](#) for further details.

(2) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad. See TI application note [SLMA002](#) for further details.

RECOMMENDED OPERATING CONDITIONS

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| Input voltage, $V_{I(IN)}$, $V_{I(INx)}$ | 2.7 | 5.5 | V |
| Input voltage, $V_{I(EN)}$, $V_{I(ENx)}$, $V_{I(EN)}$, $V_{I(ENx)}$ | 0 | 5.5 | V |
| Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$ | 0 | 500 | mA |
| Operating virtual junction temperature, T_J | -40 | 125 | °C |

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)} = 5.5$ V, $I_O = 0.5$ A, $V_{I(ENx)} = 0$ V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|--|--|---|---|--------------------------|------|------|------|
| POWER SWITCH | | | | | | | |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 5-V operation and 3.3-V operation | $V_{I(IN)} = 5$ V or 3.3 V, $I_O = 0.5$ A, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | D and DGN packages | 70 | 135 | | mΩ |
| | | | DBV package only | 95 | 140 | | |
| | | Static drain-source on-state resistance, 2.7-V operation ⁽²⁾ | $V_{I(IN)} = 2.7$ V, $I_O = 0.5$ A, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | D and DGN packages | 75 | 150 | |
| | Static drain-source on-state resistance, 5-V operation | $V_{I(IN)} = 5$ V, $I_O = 1.0$ A, OUT1 and OUT2 connected, $0^\circ\text{C} \leq T_J \leq 70^\circ\text{C}$ | DGN package, TPS2042B/52B | | | 49 | mΩ |
| t_r ⁽²⁾ | Rise time, output | $V_{I(IN)} = 5.5$ V | $C_L = 1 \mu\text{F}$, $R_L = 10 \Omega$ | $T_J = 25^\circ\text{C}$ | 0.6 | 1.5 | ms |
| | | $V_{I(IN)} = 2.7$ V | | | 0.4 | 1 | |
| t_f ⁽²⁾ | Fall time, output | $V_{I(IN)} = 5.5$ V | | | 0.05 | 0.5 | |
| | | $V_{I(IN)} = 2.7$ V | | | 0.05 | 0.5 | |
| ENABLE INPUT \overline{EN} AND \overline{ENx} | | | | | | | |
| V_{IH} | High-level input voltage | $2.7 \text{ V} \leq V_{I(IN)} \leq 5.5 \text{ V}$ | | 2 | | | V |
| V_{IL} | Low-level input voltage | $2.7 \text{ V} \leq V_{I(IN)} \leq 5.5 \text{ V}$ | | | | 0.8 | |
| I_i | Input current | $V_{I(ENx)} = 0$ V or 5.5 V | | -0.5 | | 0.5 | μA |
| t_{on} ⁽²⁾ | Turnon time | $C_L = 100 \mu\text{F}$, $R_L = 10 \Omega$ | | | | 3 | ms |
| t_{off} ⁽²⁾ | Turnoff time | $C_L = 100 \mu\text{F}$, $R_L = 10 \Omega$ | | | | 10 | |
| CURRENT LIMIT | | | | | | | |
| I_{OS} | Short-circuit output current | $V_{I(IN)} = 5$ V, OUT connected to GND, device enabled into short-circuit | $T_J = 25^\circ\text{C}$ | 0.75 | 1 | 1.25 | A |
| | | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 0.7 | 1 | 1.3 | |
| | | $V_{I(IN)} = 5$ V, OUT1 and OUT2 connected to GND, device enabled into short-circuit, measure at IN | $0^\circ\text{C} \leq T_J \leq 70^\circ\text{C}$ TPS2042B/52B | 1.5 | | | |
| SUPPLY CURRENT (TPS2041B, TPS2051B) | | | | | | | |
| Supply current, low-level output | No load on OUT, $V_{I(ENx)} = 5.5$ V, or $V_{I(ENx)} = 0$ V | $T_J = 25^\circ\text{C}$ | 0.5 | 1 | μA | | |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 0.5 | 5 | | | |
| Supply current, high-level output | No load on OUT, $V_{I(ENx)} = 0$ V, or $V_{I(ENx)} = 5.5$ V | $T_J = 25^\circ\text{C}$ | 43 | 60 | μA | | |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 43 | 70 | | | |
| Leakage current | OUT connected to ground, $V_{I(ENx)} = 5.5$ V, or $V_{I(ENx)} = 0$ V | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | 1 | μA | | |
| Reverse leakage current | $V_{I(OUTx)} = 5.5$ V, IN = ground ⁽²⁾ | $T_J = 25^\circ\text{C}$ | | 0 | μA | | |

- (1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
- (2) Not tested in production, specified by design.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating junction temperature range, $V_{I(IN)} = 5.5\text{ V}$, $I_O = 0.5\text{ A}$, $V_{I(ENx)} = 0\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|---|---|---|-----|-----|------------------|
| SUPPLY CURRENT (TPS2042B, TPS2052B) | | | | | |
| Supply current, low-level output | No load on OUT, $V_{I(\overline{ENx})} = 5.5\text{ V}$ | $T_J = 25^\circ\text{C}$ | 0.5 | 1 | μA |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 0.5 | 5 | |
| Supply current, high-level output | No load on OUT, $V_{I(\overline{ENx})} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | 50 | 70 | μA |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 50 | 90 | |
| Leakage current | OUT connected to ground, $V_{I(\overline{ENx})} = 5.5\text{ V}$ | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | 1 | μA |
| Reverse leakage current | $V_{I(OUTx)} = 5.5\text{ V}$, $I_N = \text{ground}^{(3)}$ | $T_J = 25^\circ\text{C}$ | | 0.2 | μA |
| SUPPLY CURRENT (TPS2043B, TPS2053B) | | | | | |
| Supply current, low-level output | No load on OUT, $V_{I(ENx)} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | 0.5 | 2 | μA |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 0.5 | 10 | |
| Supply current, high-level output | No load on OUT, $V_{I(ENx)} = 5.5\text{ V}$ | $T_J = 25^\circ\text{C}$ | 65 | 90 | μA |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 65 | 110 | |
| Leakage current | OUT connected to ground, $V_{I(ENx)} = 0\text{ V}$ | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | 1 | μA |
| Reverse leakage current | $V_{I(OUTx)} = 5.5\text{ V}$, $I_{Nx} = \text{ground}^{(3)}$ | $T_J = 25^\circ\text{C}$ | | 0.2 | μA |
| SUPPLY CURRENT (TPS2044B, TPS2054B) | | | | | |
| Supply current, low-level output | No load on OUT, $V_{I(\overline{ENx})} = 5.5\text{ V}$, or $V_{I(ENx)} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | 0.5 | 2 | μA |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 0.5 | 10 | |
| Supply current, high-level output | No load on OUT, $V_{I(\overline{ENx})} = 0\text{ V}$, or $V_{I(ENx)} = 5.5\text{ V}$ | $T_J = 25^\circ\text{C}$ | 75 | 110 | μA |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 75 | 140 | |
| Leakage current | OUT connected to ground, $V_{I(\overline{ENx})} = 5.5\text{ V}$, or $V_{I(ENx)} = 0\text{ V}$ | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | 1 | μA |
| Reverse leakage current | $V_{I(OUTx)} = 5.5\text{ V}$, $I_{Nx} = \text{ground}^{(3)}$ | $T_J = 25^\circ\text{C}$ | | 0.2 | μA |
| UNDERVOLTAGE LOCKOUT | | | | | |
| Low-level input voltage, I_N , I_{Nx} | | 2 | | 2.5 | V |
| Hysteresis, I_N , I_{Nx} | $T_J = 25^\circ\text{C}$ | | 75 | | mV |
| OVERCURRENT \overline{OC} and \overline{OCx} | | | | | |
| Output low voltage, $V_{OL(OCx)}$ | $I_{O(\overline{OCx})} = 5\text{ mA}$ | | | 0.4 | V |
| Off-state current ⁽³⁾ | $V_{O(\overline{OCx})} = 5\text{ V}$ or 3.3 V | | | 1 | μA |
| \overline{OC} deglitch ⁽³⁾ | \overline{OCx} assertion or deassertion | 4 | 8 | 15 | ms |
| THERMAL SHUTDOWN⁽⁴⁾ | | | | | |
| Thermal shutdown threshold ⁽³⁾ | | 135 | | | $^\circ\text{C}$ |
| Recovery from thermal shutdown ⁽³⁾ | | 125 | | | $^\circ\text{C}$ |
| Hysteresis ⁽³⁾ | | | 10 | | $^\circ\text{C}$ |

(3) Not tested in production, specified by design.

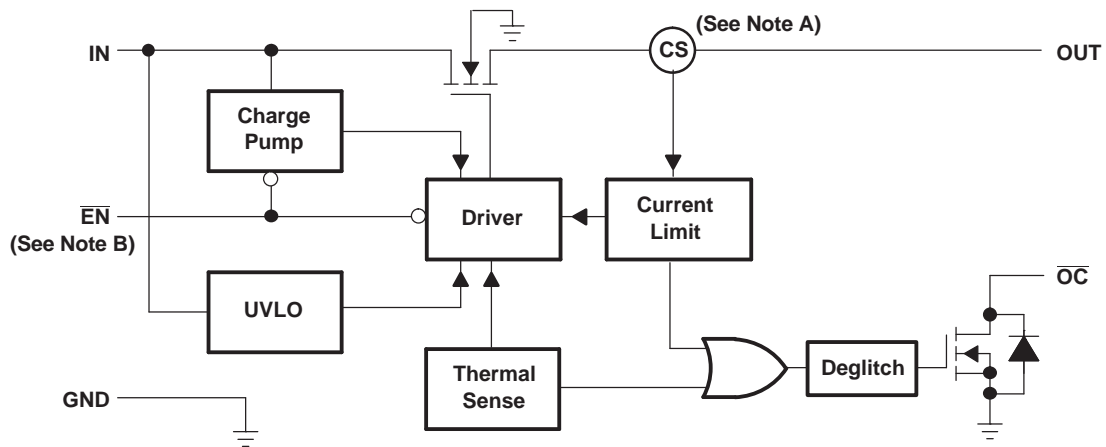
(4) The thermal shutdown only reacts under overcurrent conditions.

DEVICE INFORMATION

Terminal Functions (TPS2041B and TPS2051B)

| TERMINAL | | | | | I/O | DESCRIPTION |
|------------------------|----------|-------------|----------|----------|-----|--|
| D AND DGN PACKAGE | | DBV PACKAGE | | | | |
| NAME | TPS2041B | TPS2051B | TPS2041B | TPS2051B | | |
| $\overline{\text{EN}}$ | 4 | – | 4 | – | I | Enable input, logic low turns on power switch |
| EN | – | 4 | – | 4 | I | Enable input, logic high turns on power switch |
| GND | 1 | 1 | 2 | 2 | | Ground |
| IN | 2, 3 | 2, 3 | 5 | 5 | I | Input voltage |
| $\overline{\text{OC}}$ | 5 | 5 | 3 | 3 | O | Overcurrent open-drain output, active-low |
| OUT | 6, 7, 8 | 6, 7, 8 | 1 | 1 | O | Power-switch output |

Functional Block Diagram (TPS2041B and TPS2051B)



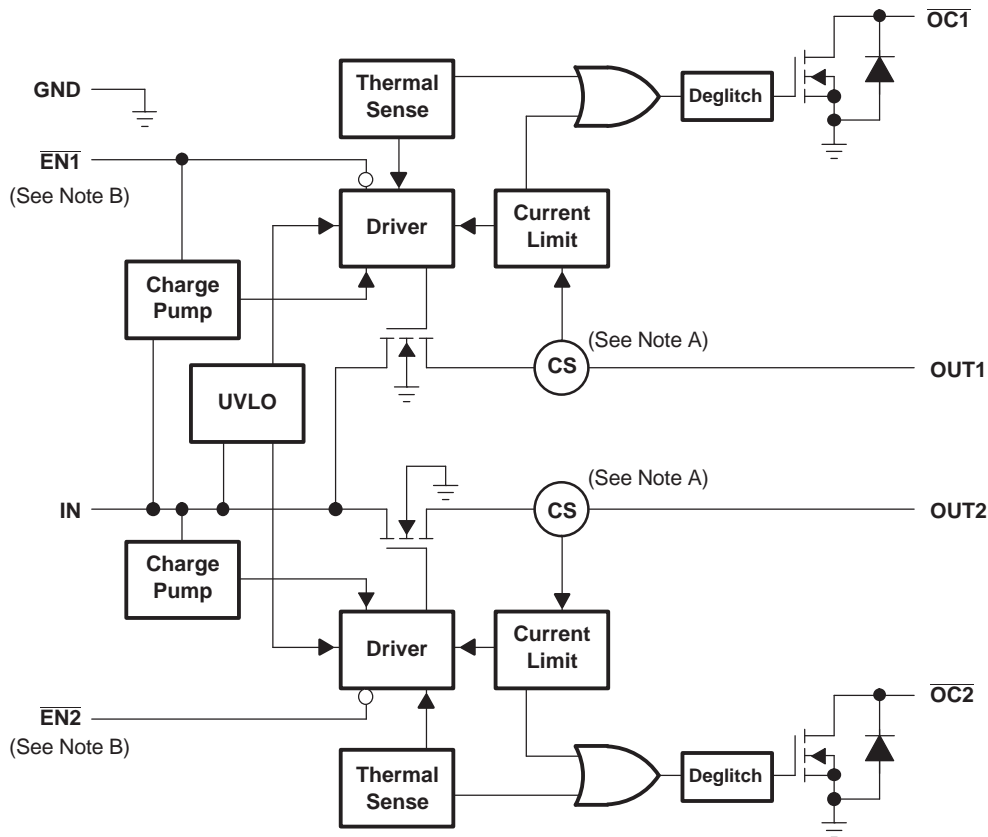
Note A: Current sense

Note B: Active low ($\overline{\text{EN}}$) for TPS2041B; Active high (EN) for TPS2051B

Terminal Functions (TPS2042B and TPS2052B)

| TERMINAL | | | I/O | DESCRIPTION |
|--------------------------|----------|----------|-----|--|
| D, DGN, and DRB PACKAGES | | | | |
| NAME | TPS2042B | TPS2052B | | |
| $\overline{\text{EN1}}$ | 3 | - | I | Enable input, logic low turns on power switch IN-OUT1 |
| $\overline{\text{EN2}}$ | 4 | - | I | Enable input, logic low turns on power switch IN-OUT2 |
| EN1 | - | 3 | I | Enable input, logic high turns on power switch IN-OUT1 |
| EN2 | - | 4 | I | Enable input, logic high turns on power switch IN-OUT2 |
| GND | 1 | 1 | | Ground |
| IN | 2 | 2 | I | Input voltage |
| $\overline{\text{OC1}}$ | 8 | 8 | O | Overcurrent, open-drain output, active low, IN-OUT1 |
| $\overline{\text{OC2}}$ | 5 | 5 | O | Overcurrent, open-drain output, active low, IN-OUT2 |
| OUT1 | 7 | 7 | O | Power-switch output, IN-OUT1 |
| OUT2 | 6 | 6 | O | Power-switch output, IN-OUT2 |
| PowerPAD™ | - | - | | Internally connected to GND; used to heat-sink the part to the circuit board traces. Should be connected to GND pin. |

Functional Block Diagram (TPS2042B and TPS2052B)



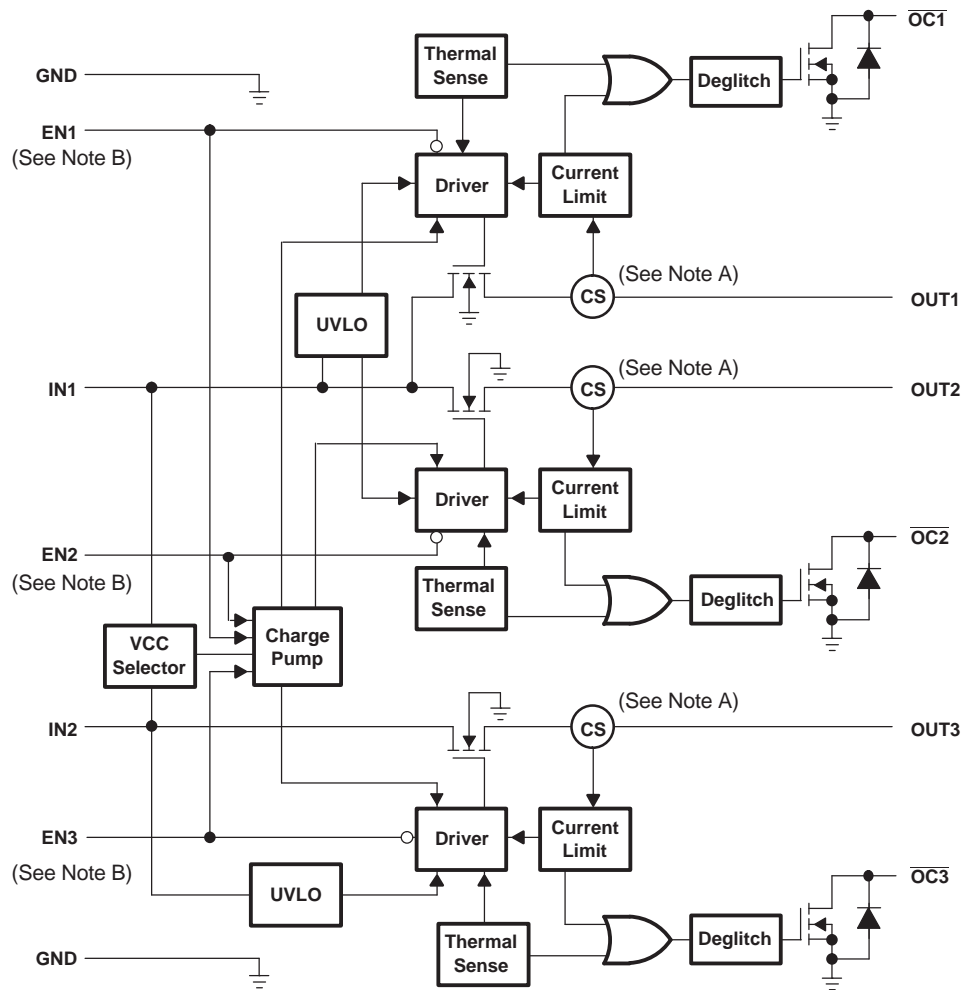
Note A: Current sense

Note B: Active low ($\overline{\text{ENx}}$) for TPS2042B; Active high (ENx) for TPS2052B

Terminal Functions (TPS2043B and TPS2053B)

| NAME | TERMINAL | | I/O | DESCRIPTION |
|-------------------------|----------|----------|-----|---|
| | TPS2043B | TPS2053B | | |
| $\overline{\text{EN1}}$ | 3 | -- | I | Enable input, logic low turns on power switch IN1-OUT1 |
| $\overline{\text{EN2}}$ | 4 | -- | I | Enable input, logic low turns on power switch IN1-OUT2 |
| $\overline{\text{EN3}}$ | 7 | -- | I | Enable input, logic low turns on power switch IN2-OUT3 |
| EN1 | -- | 3 | I | Enable input, logic high turns on power switch IN1-OUT1 |
| EN2 | -- | 4 | I | Enable input, logic high turns on power switch IN1-OUT2 |
| EN3 | -- | 7 | I | Enable input, logic high turns on power switch IN2-OUT3 |
| GND | 1, 5 | 1, 5 | | Ground |
| IN1 | 2 | 2 | I | Input voltage for OUT1 and OUT2 |
| IN2 | 6 | 6 | I | Input voltage for OUT3 |
| NC | 8, 9, 10 | 8, 9, 10 | | No connection |
| $\overline{\text{OC1}}$ | 16 | 16 | O | Overcurrent, open-drain output, active low, IN1-OUT1 |
| $\overline{\text{OC2}}$ | 13 | 13 | O | Overcurrent, open-drain output, active low, IN1-OUT2 |
| $\overline{\text{OC3}}$ | 12 | 12 | O | Overcurrent, open-drain output, active low, IN2-OUT3 |
| OUT1 | 15 | 15 | O | Power-switch output, IN1-OUT1 |
| OUT2 | 14 | 14 | O | Power-switch output, IN1-OUT2 |
| OUT3 | 11 | 11 | O | Power-switch output, IN2-OUT3 |

Functional Block Diagram (TPS2043B and TPS2053B)



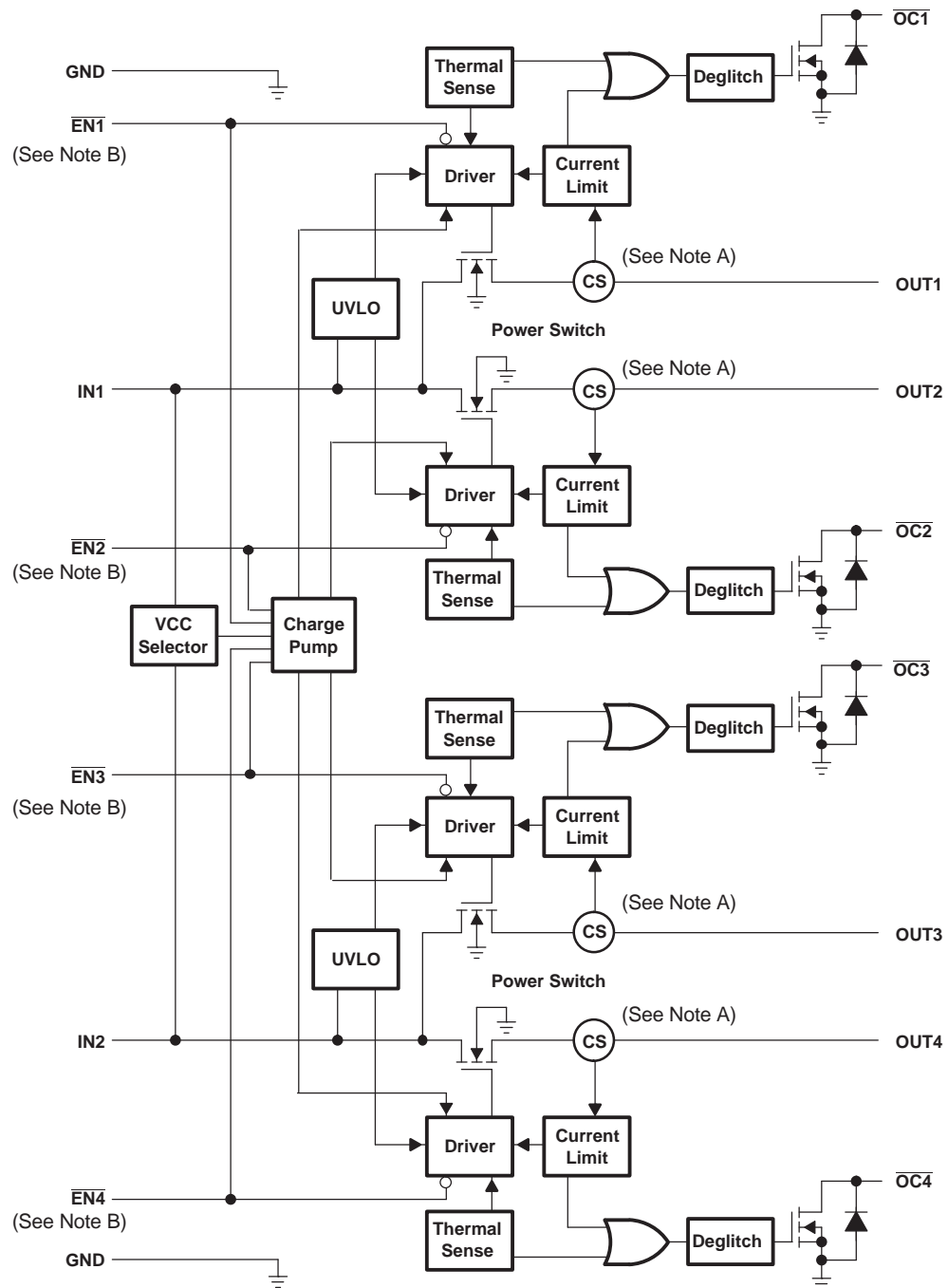
Note A: Current sense

Note B: Active low (\overline{ENx}) for TPS2043B; Active high (ENx) for TPS2053B

Terminal Functions (TPS2044B and TPS2054B)

| NAME | TERMINAL | | I/O | DESCRIPTION |
|-------------------------|----------|----------|-----|---|
| | TPS2044B | TPS2054B | | |
| $\overline{\text{EN1}}$ | 3 | - | I | Enable input, logic low turns on power switch IN1-OUT1 |
| $\overline{\text{EN2}}$ | 4 | - | I | Enable input, logic low turns on power switch IN1-OUT2 |
| $\overline{\text{EN3}}$ | 7 | - | I | Enable input, logic low turns on power switch IN2-OUT3 |
| $\overline{\text{EN4}}$ | 8 | - | I | Enable input, logic low turns on power switch IN2-OUT4 |
| EN1 | - | 3 | I | Enable input, logic high turns on power switch IN1-OUT1 |
| EN2 | - | 4 | I | Enable input, logic high turns on power switch IN1-OUT2 |
| EN3 | - | 7 | I | Enable input, logic high turns on power switch IN2-OUT3 |
| EN4 | - | 8 | I | Enable input, logic high turns on power switch IN2-OUT4 |
| GND | 1, 5 | 1, 5 | | Ground |
| IN1 | 2 | 2 | I | Input voltage for OUT1 and OUT2 |
| IN2 | 6 | 6 | I | Input voltage for OUT3 and OUT4 |
| $\overline{\text{OC1}}$ | 16 | 16 | O | Overcurrent, open-drain output, active low, IN1-OUT1 |
| $\overline{\text{OC2}}$ | 13 | 13 | O | Overcurrent, open-drain output, active low, IN1-OUT2 |
| $\overline{\text{OC3}}$ | 12 | 12 | O | Overcurrent, open-drain output, active low, IN2-OUT3 |
| $\overline{\text{OC4}}$ | 9 | 9 | O | Overcurrent, open-drain output, active low, IN2-OUT4 |
| OUT1 | 15 | 15 | O | Power-switch output, IN1-OUT1 |
| OUT2 | 14 | 14 | O | Power-switch output, IN1-OUT2 |
| OUT3 | 11 | 11 | O | Power-switch output, IN2-OUT3 |
| OUT4 | 10 | 10 | O | Power-switch output, IN2-OUT4 |

Functional Block Diagram (TPS2044B and TPS2054B)



Note A: Current sense

Note B: Active low (\overline{ENx}) for TPS2044B; Active high (ENx) for TPS2054B

PARAMETER MEASUREMENT INFORMATION

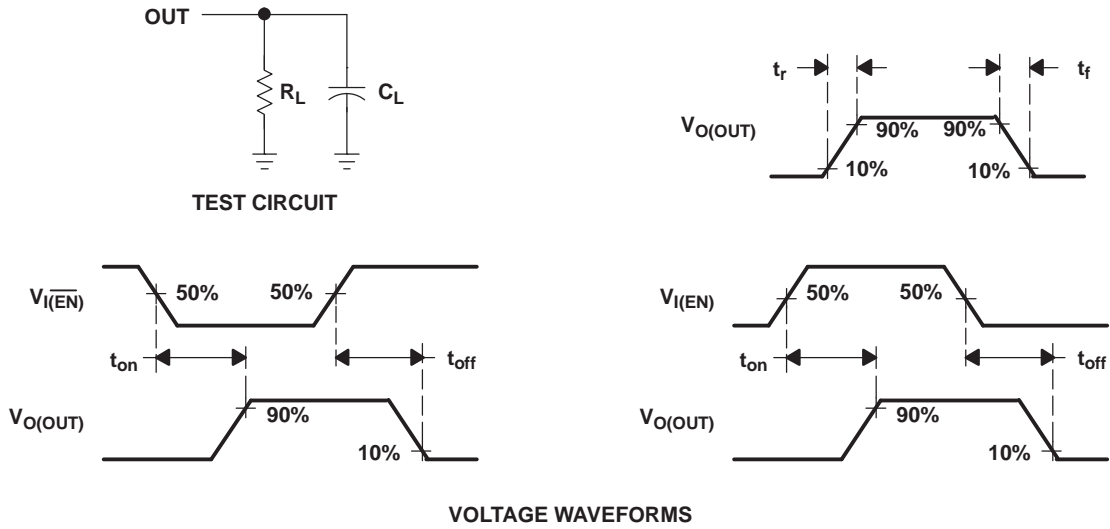


Figure 1. Test Circuit and Voltage Waveforms

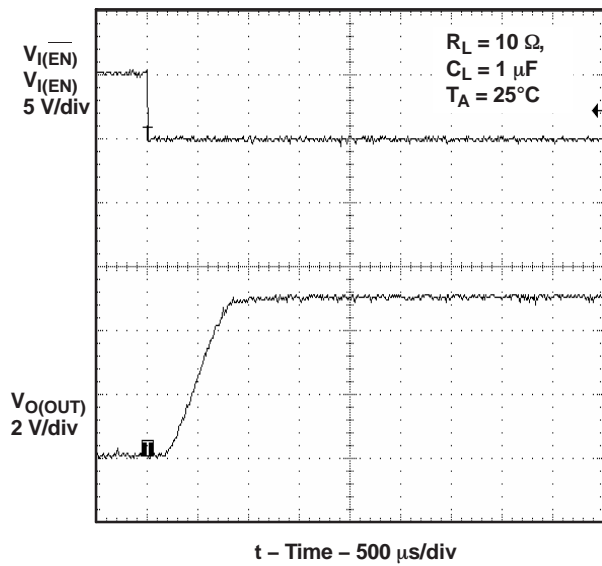


Figure 2. Turnon Delay and Rise Time With 1- μF Load

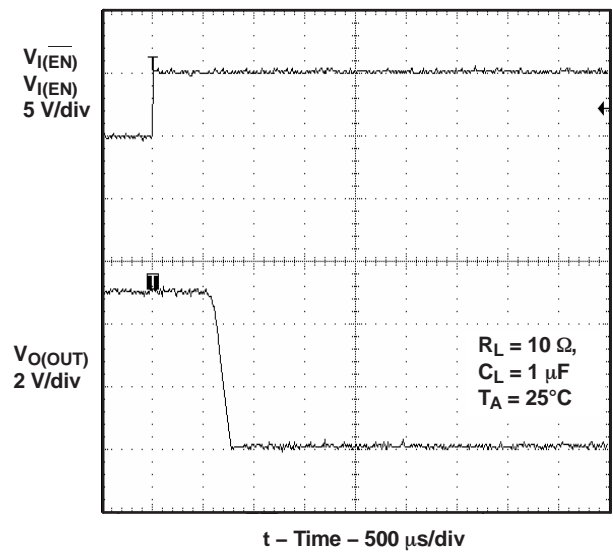


Figure 3. Turnoff Delay and Fall Time With 1- μF Load

PARAMETER MEASUREMENT INFORMATION (continued)

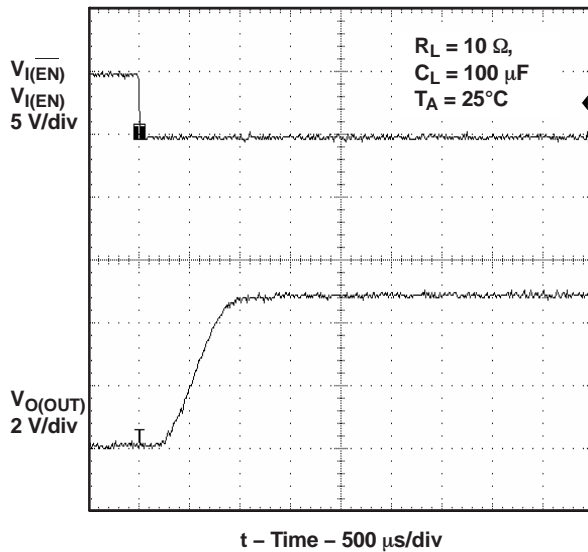


Figure 4. Turnon Delay and Rise Time With 100- μF Load

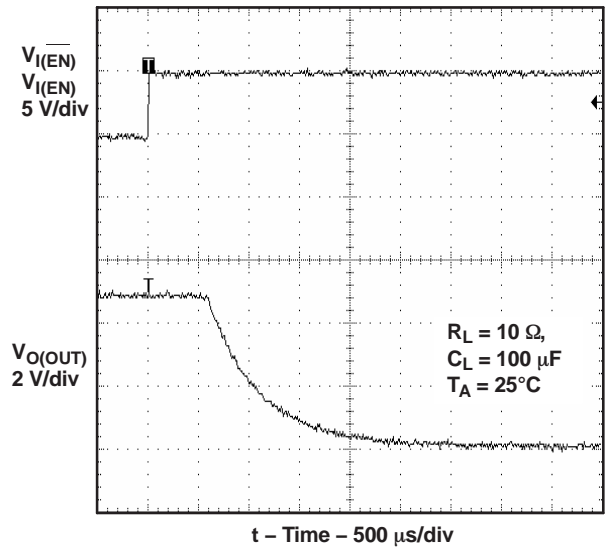


Figure 5. Turnoff Delay and Fall Time With 100- μF Load

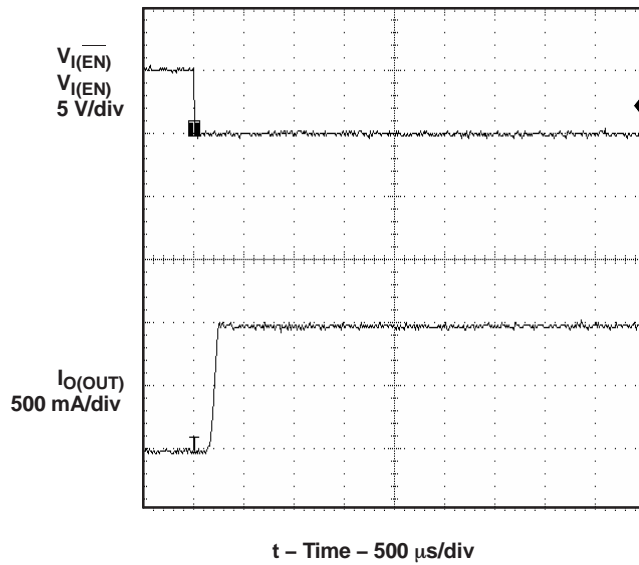


Figure 6. Short-Circuit Current, Device Enabled Into Short

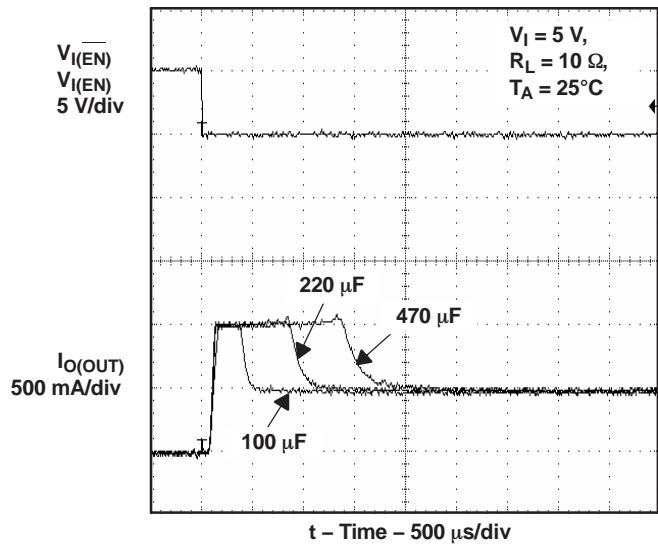
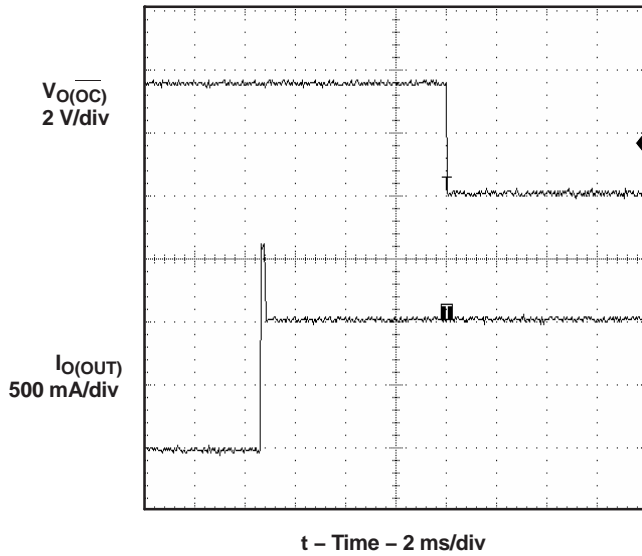


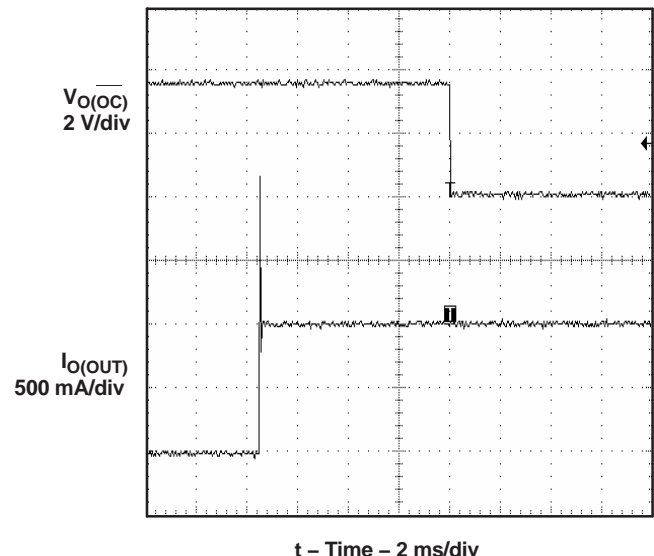
Figure 7. Inrush Current With Different Load Capacitance

PARAMETER MEASUREMENT INFORMATION (continued)



t – Time – 2 ms/div

Figure 8. 3-Ω Load Connected to Enabled Device



t – Time – 2 ms/div

Figure 9. 2-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

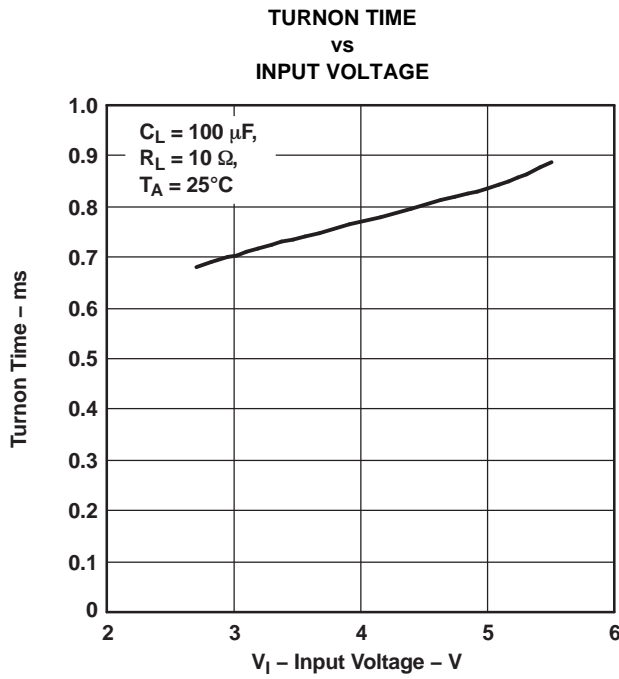


Figure 10.

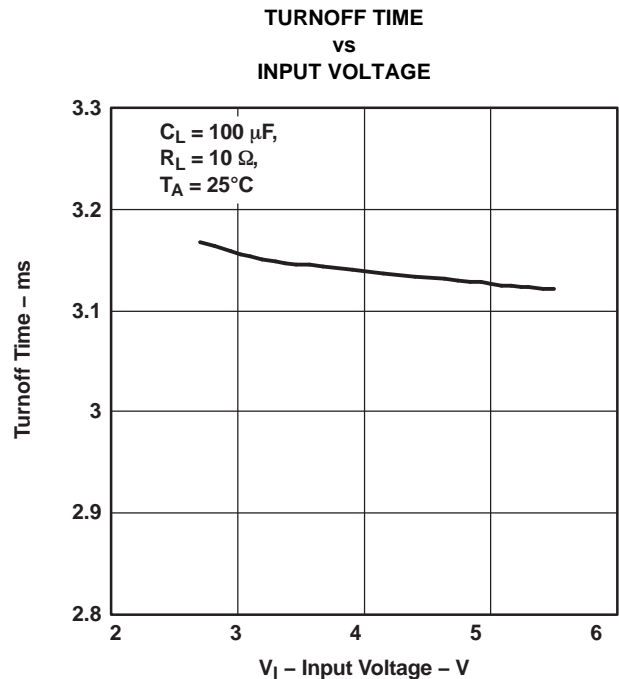


Figure 11.

TYPICAL CHARACTERISTICS (continued)

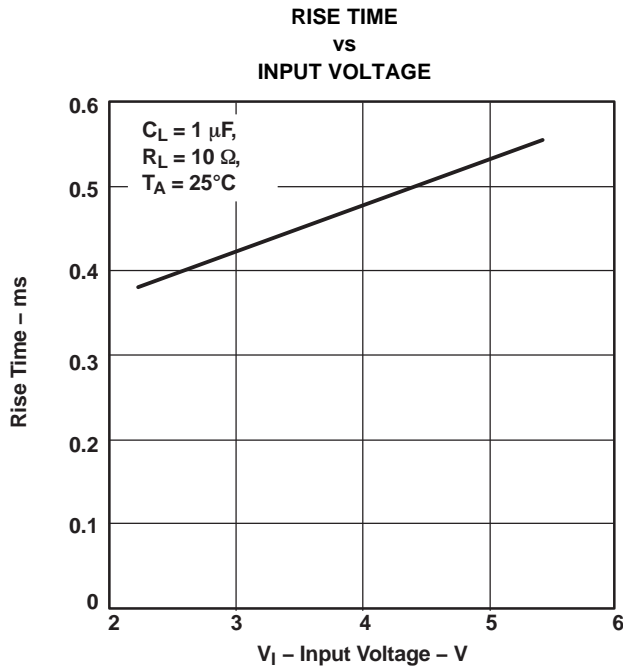


Figure 12.

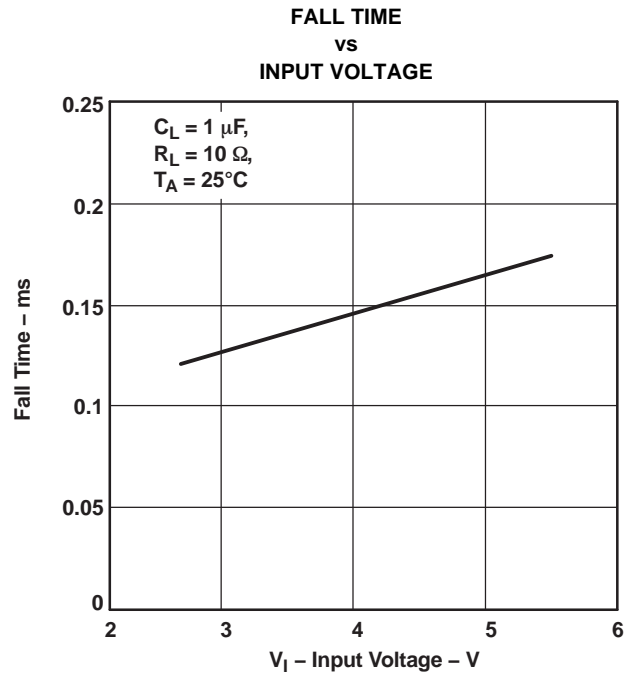


Figure 13.

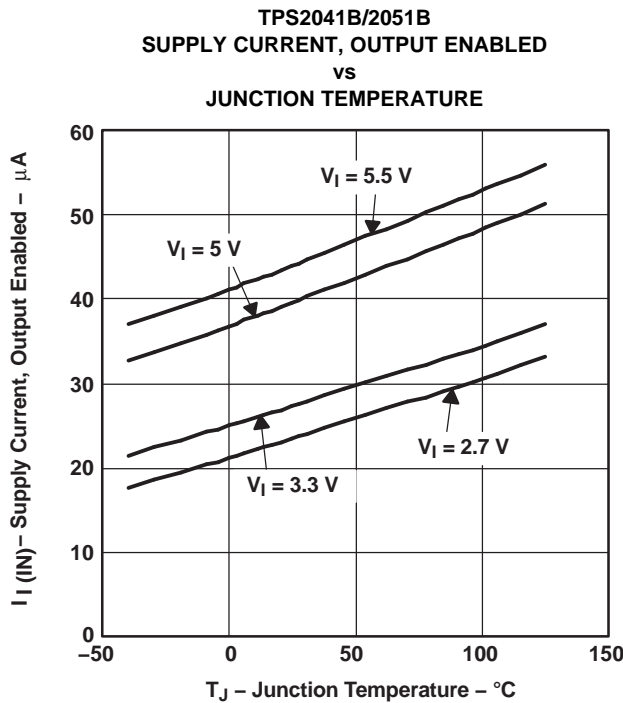


Figure 14.

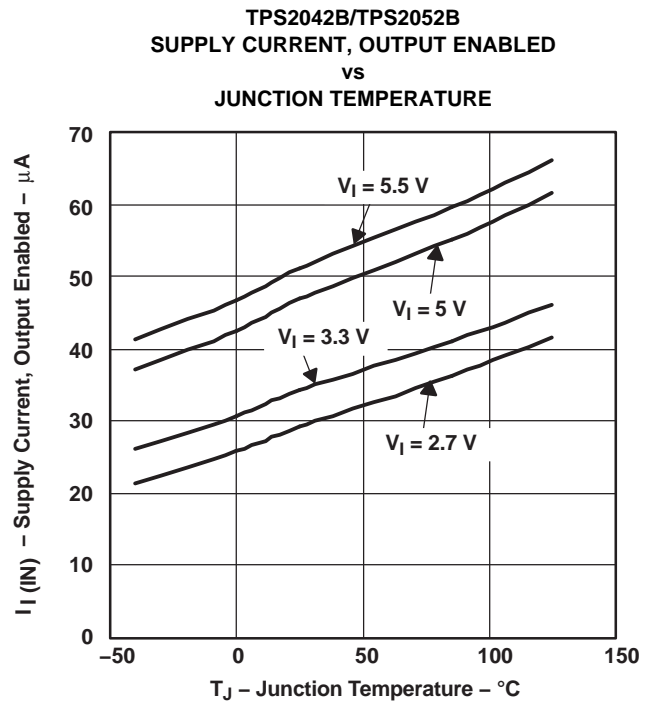


Figure 15.

TYPICAL CHARACTERISTICS (continued)

TPS2043B/TPS2053B
 SUPPLY CURRENT, OUTPUT ENABLED
 vs
 JUNCTION TEMPERATURE

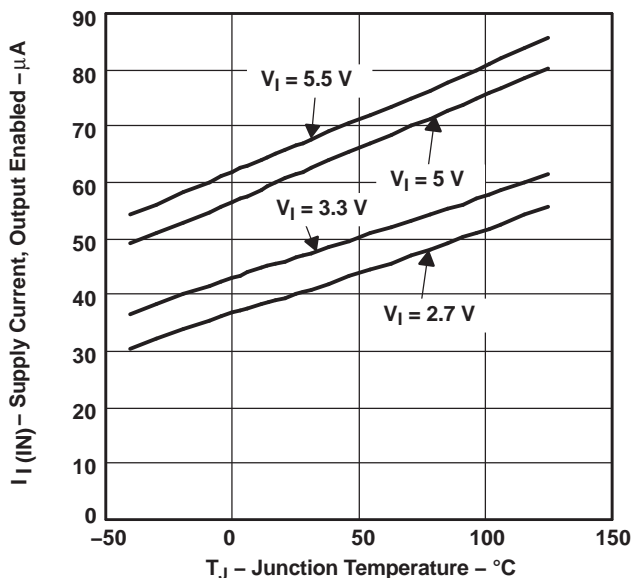


Figure 16.

TPS2044B/TPS2054B
 SUPPLY CURRENT, OUTPUT ENABLED
 vs
 JUNCTION TEMPERATURE

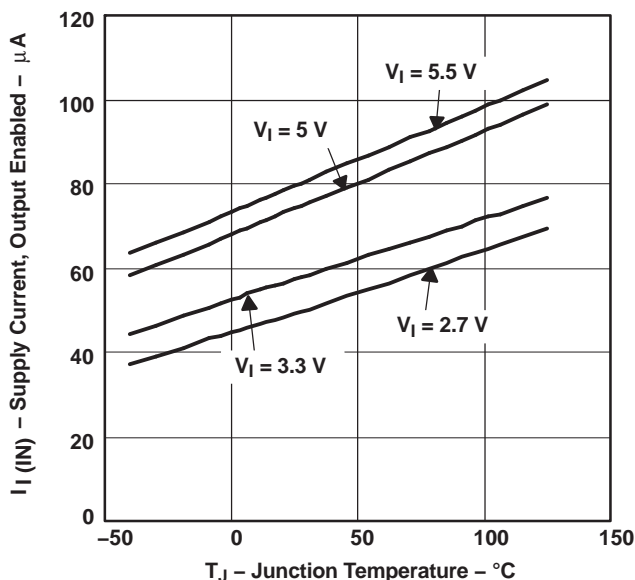


Figure 17.

TPS2041B/TPS2051B
 SUPPLY CURRENT, OUTPUT DISABLED
 vs
 JUNCTION TEMPERATURE

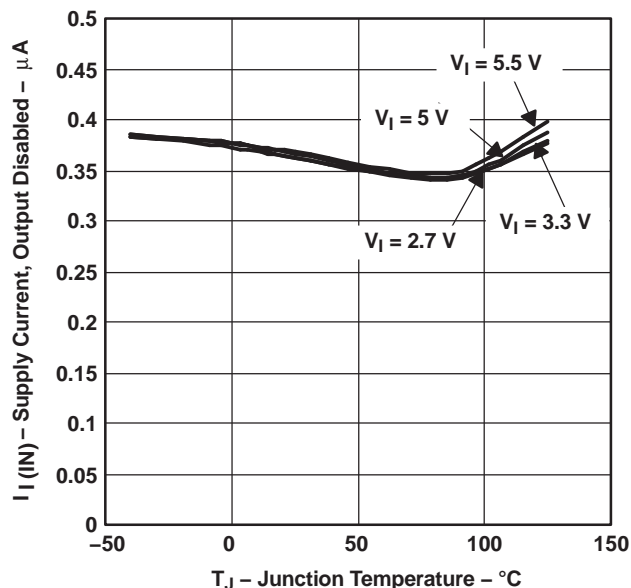


Figure 18.

TPS2042B/TPS2052B
 SUPPLY CURRENT, OUTPUT DISABLED
 vs
 JUNCTION TEMPERATURE

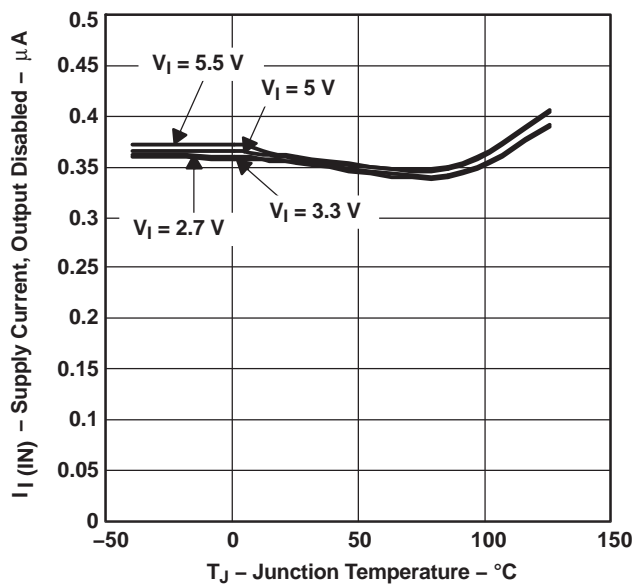


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TPS2043B/TPS2053B
 SUPPLY CURRENT, OUTPUT DISABLED
 vs
 JUNCTION TEMPERATURE

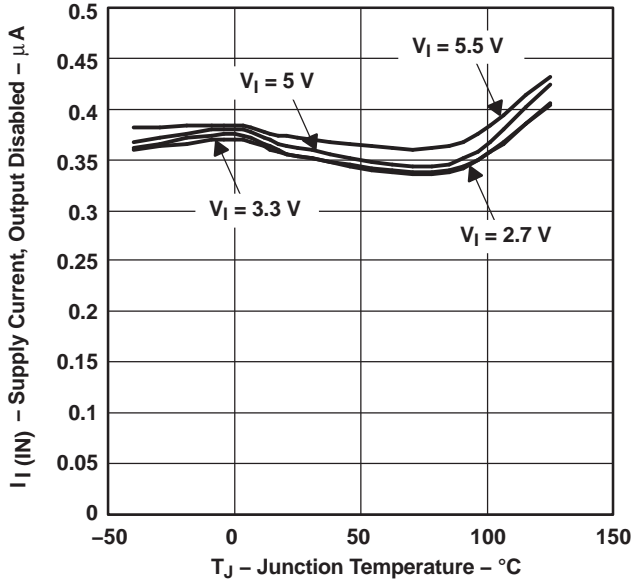


Figure 20.

TPS2044B/TPS2054B
 SUPPLY CURRENT, OUTPUT DISABLED
 vs
 JUNCTION TEMPERATURE

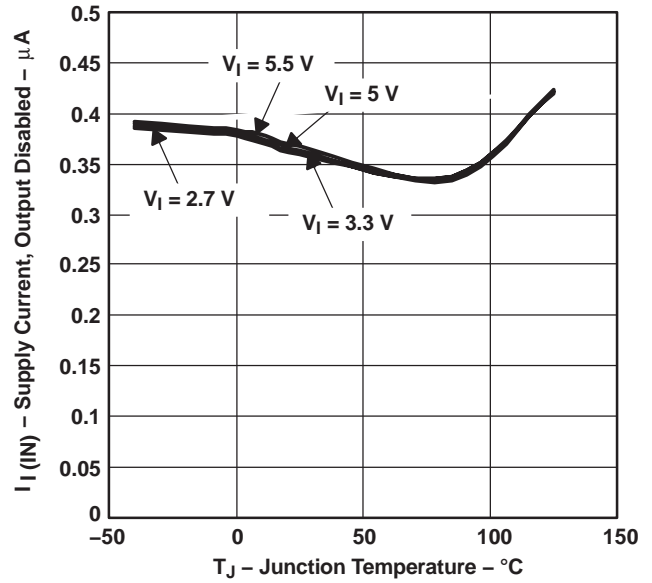


Figure 21.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
 vs
 JUNCTION TEMPERATURE

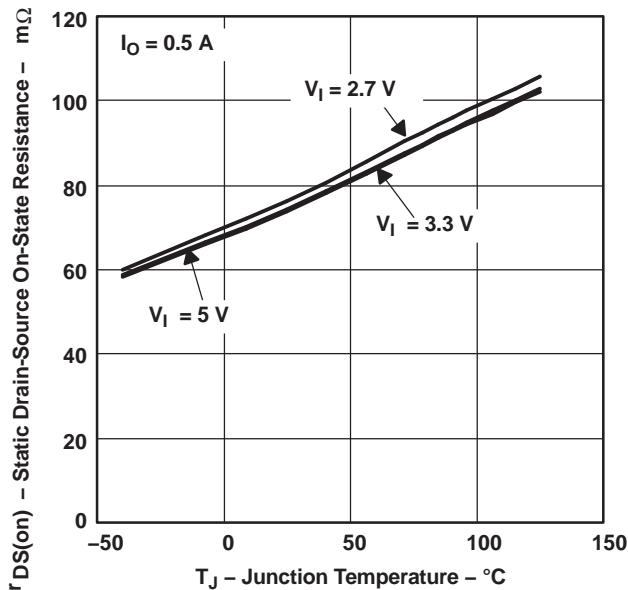


Figure 22.

SHORT-CIRCUIT OUTPUT CURRENT
 vs
 JUNCTION TEMPERATURE

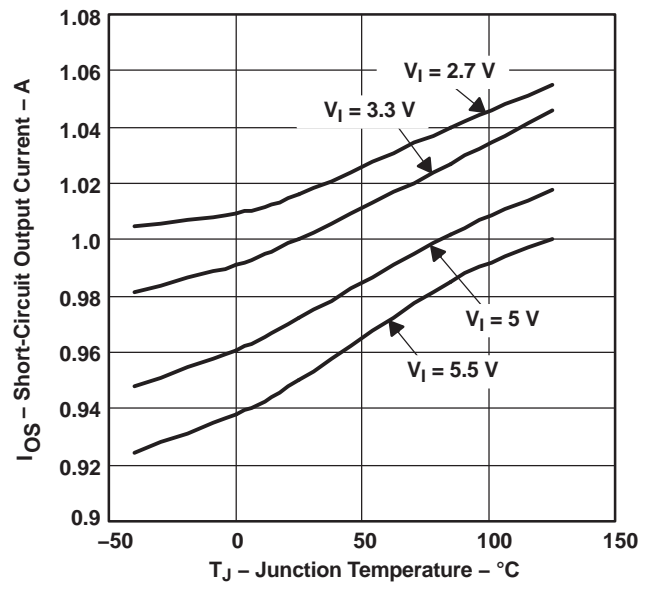


Figure 23.

TYPICAL CHARACTERISTICS (continued)

THRESHOLD TRIP CURRENT
 vs
 INPUT VOLTAGE

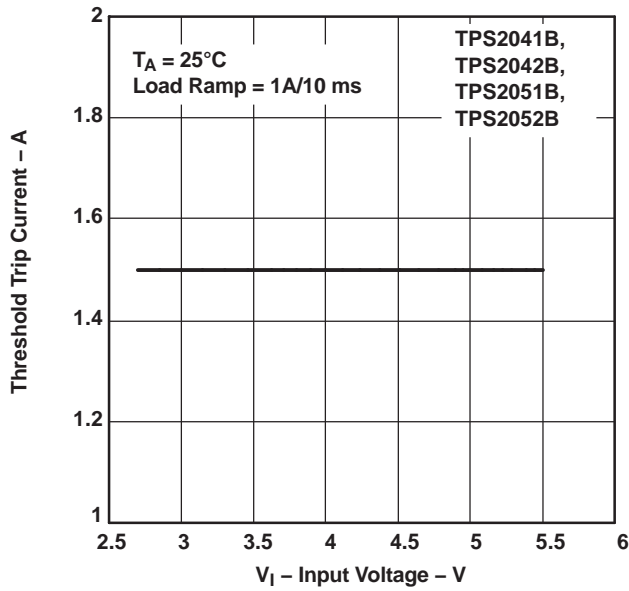


Figure 24.

THRESHOLD TRIP CURRENT
 vs
 INPUT VOLTAGE

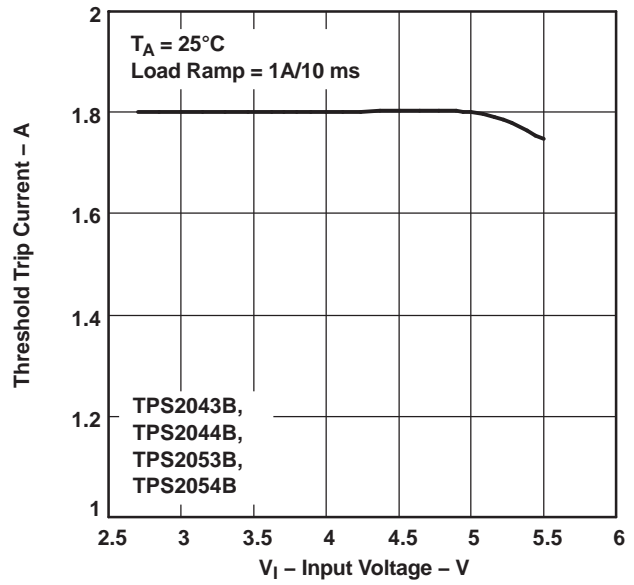


Figure 25.

UNDERVOLTAGE LOCKOUT
 vs
 JUNCTION TEMPERATURE

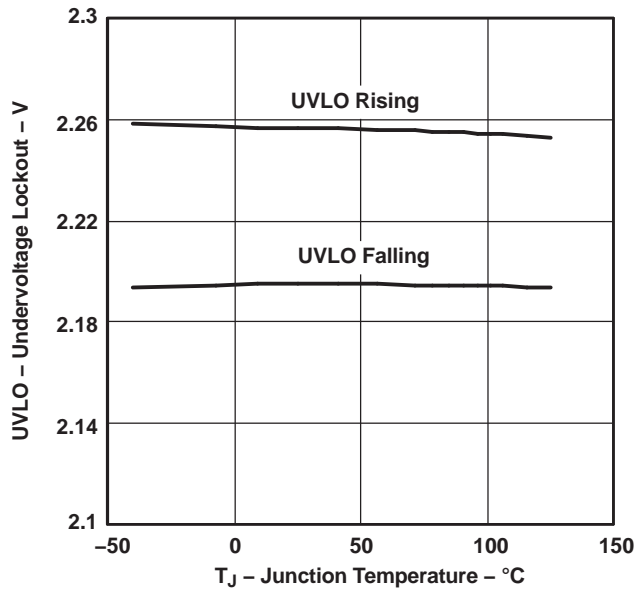


Figure 26.

CURRENT-LIMIT RESPONSE
 vs
 PEAK CURRENT

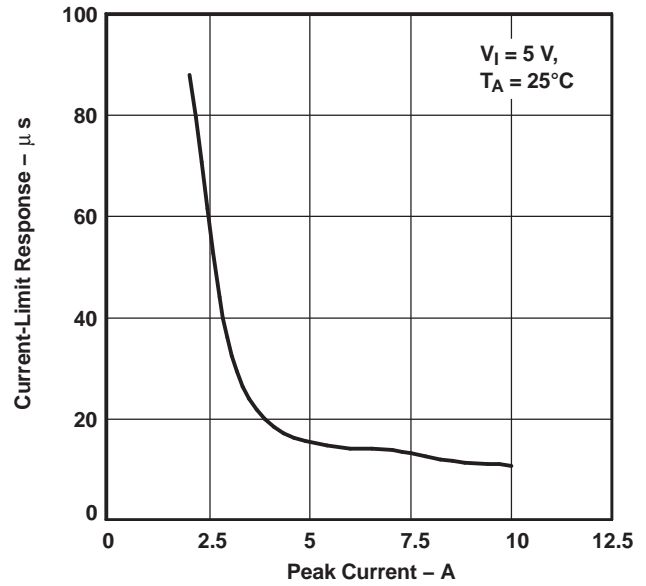


Figure 27.

APPLICATION INFORMATION

POWER-SUPPLY CONSIDERATIONS

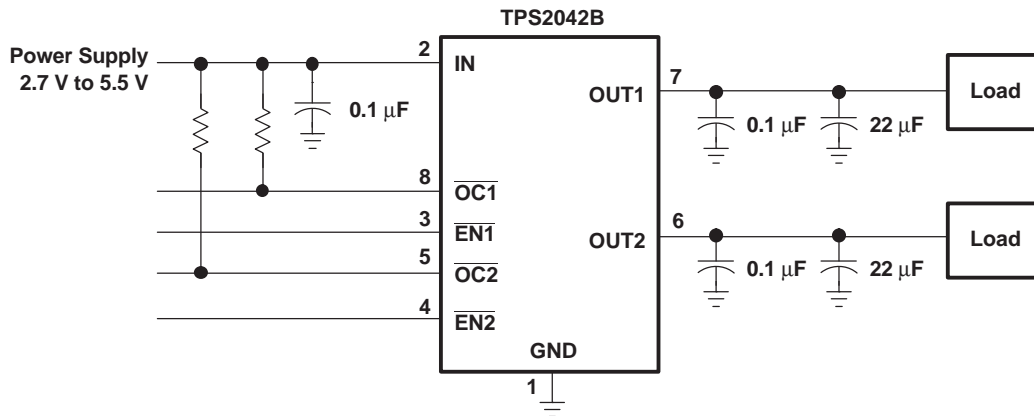


Figure 28. Typical Application (Example, TPS2042B)

A 0.01- μF to 0.1- μF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- μF to 0.1- μF ceramic capacitor improves the immunity of the device to short-circuit transients.

OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 14 through Figure 17). The TPS204xB/TPS205xB senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 18 through Figure 21). The TPS204xB/TPS205xB is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ RESPONSE

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{\text{OCx}}$ occurs due to the 10-ms deglitch circuit. The TPS204xB/TPS205xB is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{\text{OCx}}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

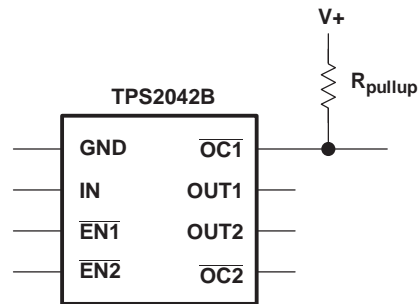


Figure 29. Typical Circuit for the \overline{OC} Pin (Example, TPS2042B)

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from [Figure 22](#). Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature °C

$R_{\theta JA}$ = Thermal resistance

P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS204xB/TPS205xB implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The \overline{OCx} open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS204xB/TPS205xB can provide-power distribution solutions to many of these classes of devices.

HOST/SELF-POWERED AND BUS-POWERED HUBS

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see [Figure 30](#) and [Figure 31](#)). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

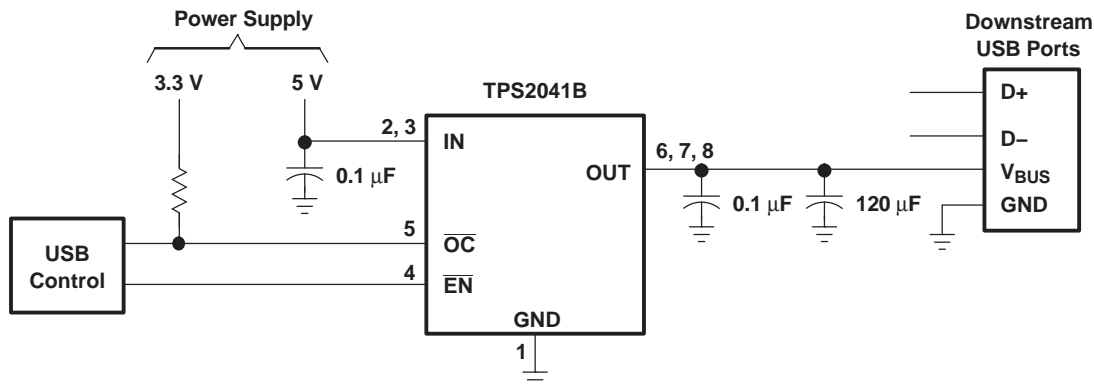


Figure 30. Typical One-Port USB Host / Self-Powered Hub

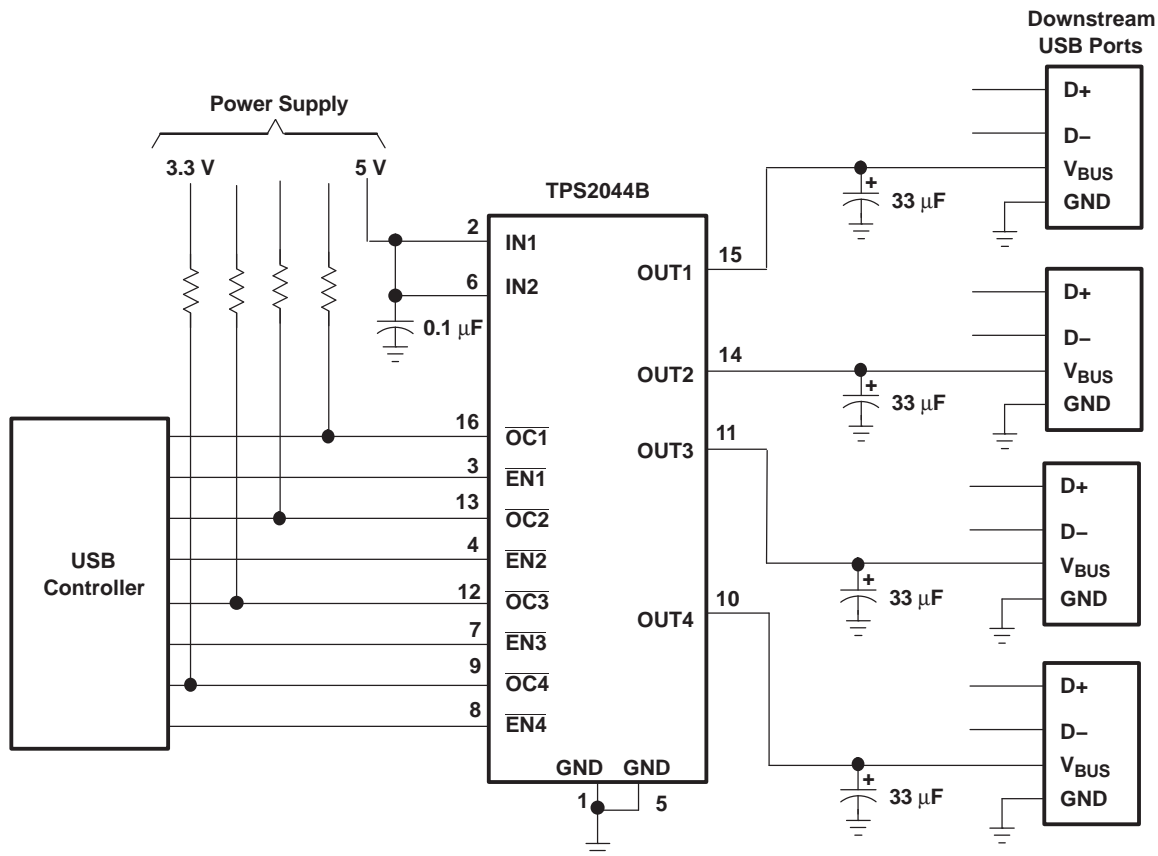


Figure 31. Typical Four-Port USB Host / Self-Powered Hub

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 32).

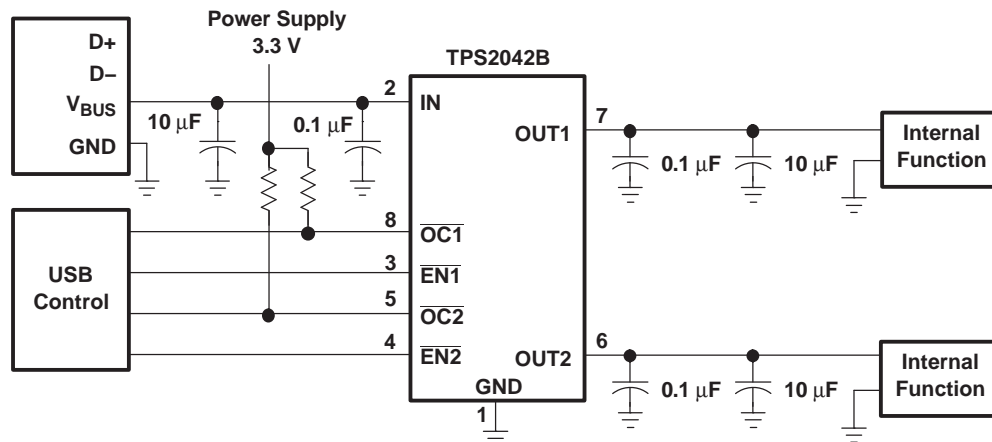


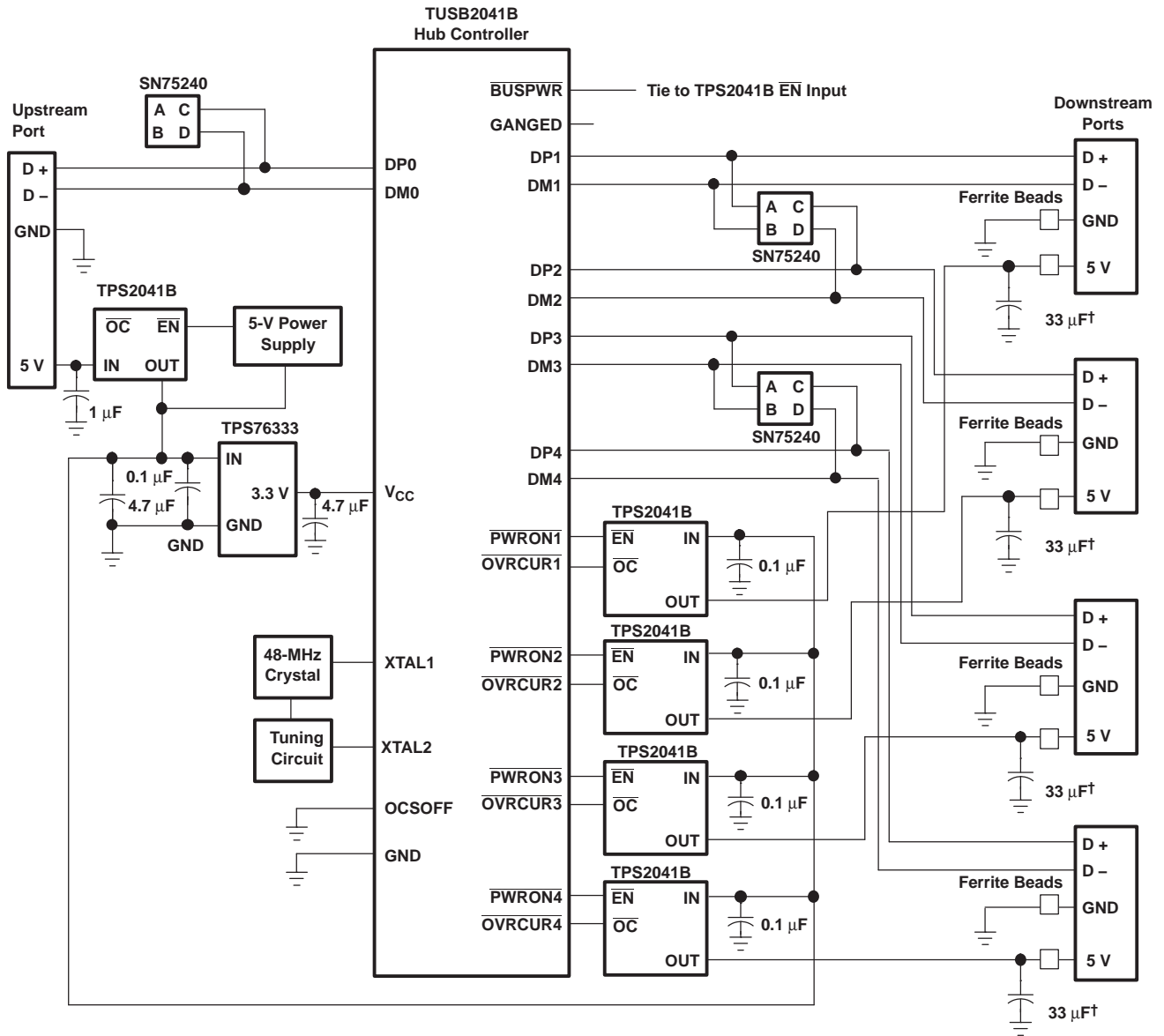
Figure 32. High-Power Bus-Powered Function (Example, TPS2042B)

USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

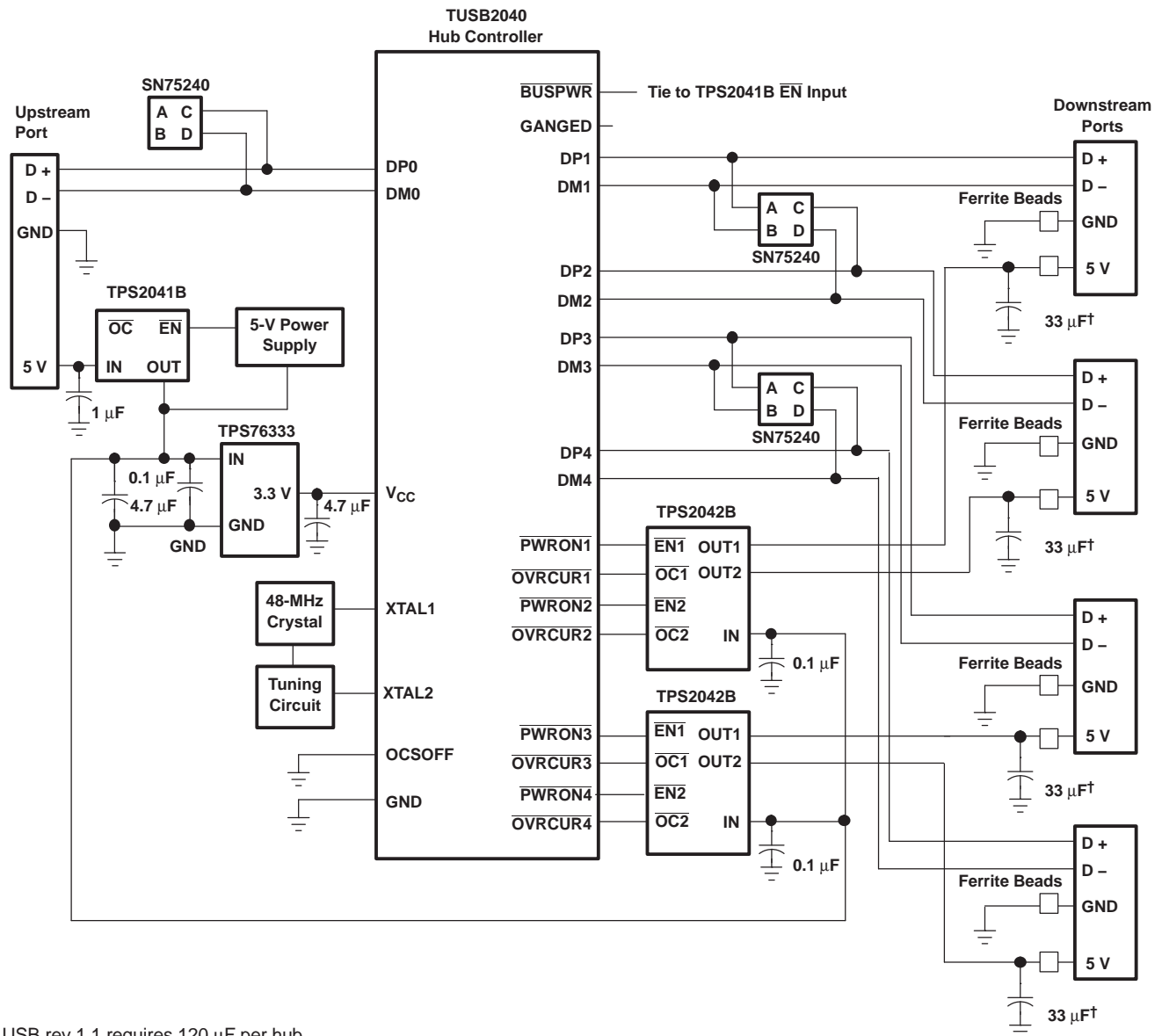
- Hosts/self-powered hubs must:
 - Current-limit downstream ports
 - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
 - Enable/disable power to downstream ports
 - Power up at <100 mA
 - Limit inrush current (<44 Ω and 10 μ F)
- Functions must:
 - Limit inrush currents
 - Power up at <100 mA

The feature set of the TPS204xB/TPS205xB allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see [Figure 33](#) through [Figure 36](#)).



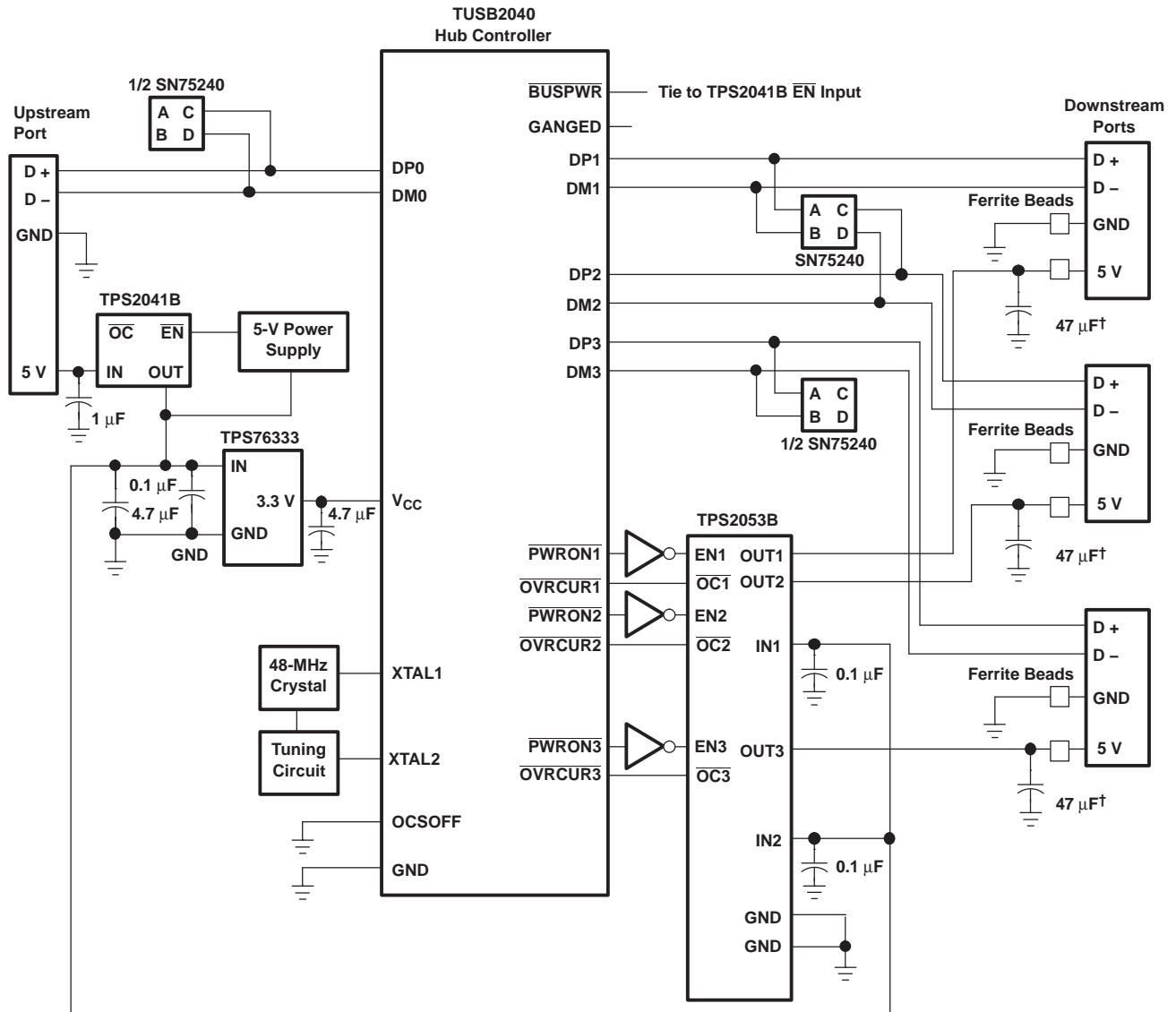
† USB rev 1.1 requires 120 µF per hub.

Figure 33. Hybrid Self / Bus-Powered Hub Implementation, TPS2041B/TPS2051B



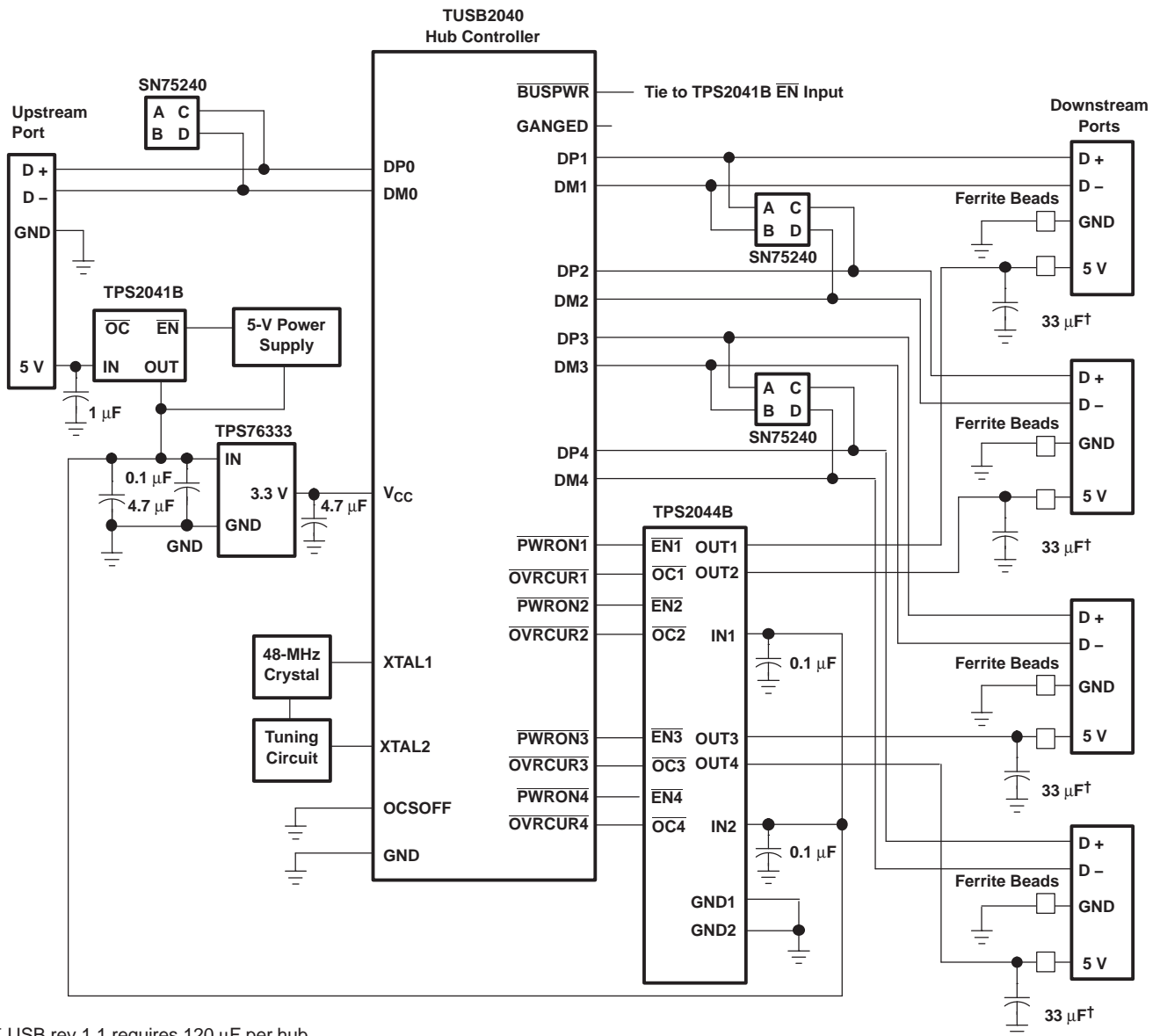
† USB rev 1.1 requires 120 μF per hub.

Figure 34. Hybrid Self / Bus-Powered Hub Implementation, TPS2042B/TPS2052B



† USB rev 1.1 requires 120 µF per hub.

Figure 35. Hybrid Self / Bus-Powered Hub Implementation, TPS2043B/TPS2053B



† USB rev 1.1 requires 120 μF per hub.

Figure 36. Hybrid Self / Bus-Powered Hub Implementation, TPS2044B/TPS2054B

GENERIC HOT-PLUG APPLICATIONS

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS204xB/TPS205xB, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS204xB/TPS205xB also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

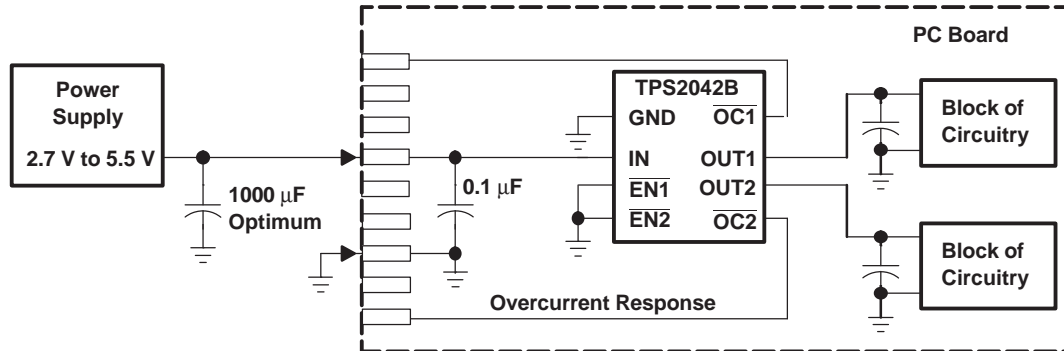


Figure 37. Typical Hot-Plug Implementation (Example, TPS2042B)

By placing the TPS204xB/TPS205xB between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

DETAILED DESCRIPTION

Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 500 mA.

Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

Enable (\overline{ENx})

The logic enable pin disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 μ A or 2 μ A when a logic high is present on \overline{EN} . A logic zero input on \overline{EN} restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

Enable (ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 μA or 2 μA when a logic low is present on ENx. A logic high input on ENx restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

Overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{\text{OCx}}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{\text{OCx}}$ is asserted instantaneously.

Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

Thermal Sense

The TPS204xB/TPS205xB implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{\text{OCx}}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

REVISION HISTORY

| Changes from Revision F (June 2006) to Revision G | Page |
|--|-------------|
| • Deleted Product Preview from the DBV package | 1 |
| • Added TPS2060 1.5 A and TPS2064 1.5 A to the General Switch Catalog table | 1 |
| • Added DRB package to the Ordering Information table | 2 |
| • Added D, DGN and DBV package options to the $r_{DS(on)}$ Test Condition | 3 |
| • Added the DBV PACKAGE to the Terminal Functions table | 5 |
| <hr/> | |
| Changes from Revision G (OCTOBER 2006) to Revision H | Page |
| • Updated the General Switch Catalog table | 1 |
| <hr/> | |
| Changes from Revision H (September 2007) to Revision I | Page |
| • Added Featured Bullet: Additional UL Recognition.. | 1 |
| • Added DRB-8 pinout package. | 1 |
| • Added DRB-8 to the Dissipation Rating Table. | 2 |
| <hr/> | |
| Changes from Revision I (October 2008) to Revision J | Page |
| • Deleted Product Preview from the DRB package | 1 |
| • Deleted Electrical Char Table note - This configuration has not been tested for UL certification. | 4 |
| <hr/> | |
| Changes from Revision J (December 2008) to Revision K | Page |
| • Deleted Electrical Char Table note - Estimated value. Final value pending characterization. | 4 |

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|-------------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|--|
| TPS2041BD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2041BDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2041BDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2041BDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2041BDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2041BDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2041BDGN | ACTIVE | MSOP- PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2041BDGN-ASY | OBSOLETE | MSOP- PowerPAD | DGN | 8 | | TBD | Call TI | Call TI | Samples Not Available |
| TPS2041BDGNG4 | ACTIVE | MSOP- PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2041BDGNR | ACTIVE | MSOP- PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2041BDGNRG4 | ACTIVE | MSOP- PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2041BDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Alternative Sample TPS2041BD |
| TPS2041BDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2042BD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2042BDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2042BDGN | ACTIVE | MSOP- PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2042BDGNG4 | ACTIVE | MSOP- PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|-------------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|--------------------------------------|
| TPS2042BDGNR | ACTIVE | MSOP- PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2042BDGNRG4 | ACTIVE | MSOP- PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2042BDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2042BDRBR | ACTIVE | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2042BDRBT | ACTIVE | SON | DRB | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2042BDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2043BD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2043BDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2043BDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2043BDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2044BD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2044BDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2044BDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2044BDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2051BD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2051BDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2051BDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2051BDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|-------------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|--------------------------------------|
| TPS2051BDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2051BDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2051BDGN | ACTIVE | MSOP- PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2051BDGNG4 | ACTIVE | MSOP- PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2051BDGNR | ACTIVE | MSOP- PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2051BDGNRG4 | ACTIVE | MSOP- PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2051BDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2051BDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2052BD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2052BDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2052BDGN | ACTIVE | MSOP- PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2052BDGNG4 | ACTIVE | MSOP- PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2052BDGNR | ACTIVE | MSOP- PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2052BDGNRG4 | ACTIVE | MSOP- PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2052BDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2052BDRBR | ACTIVE | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2052BDRBT | ACTIVE | SON | DRB | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2052BDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|--------------------------------------|
| TPS2053BD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2053BDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2053BDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2053BDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2054BD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2054BDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| TPS2054BDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |
| TPS2054BDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Request Free Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

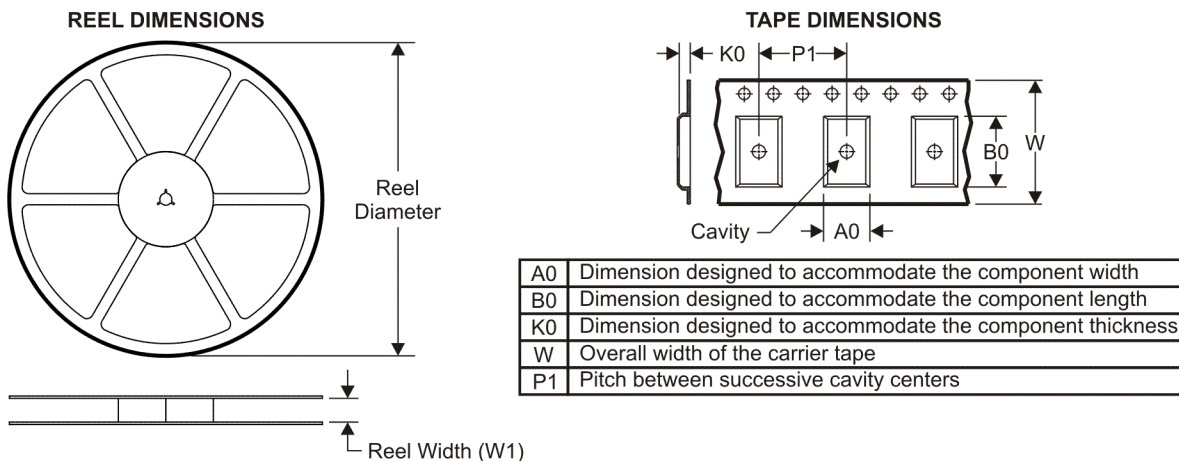
OTHER QUALIFIED VERSIONS OF TPS2041B, TPS2042B, TPS2051B :

- Automotive: [TPS2041B-Q1](#), [TPS2042B-Q1](#), [TPS2051B-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



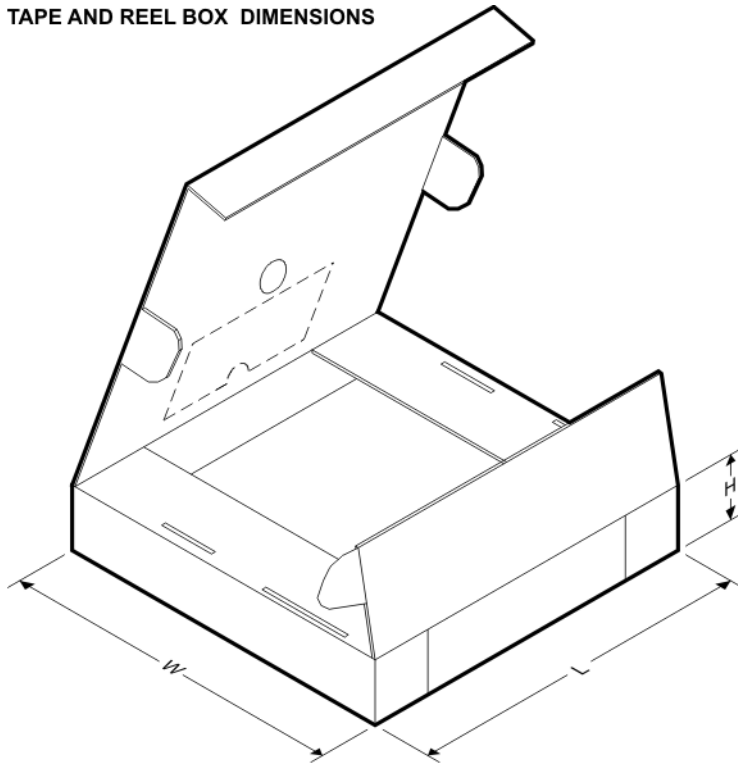
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|----------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2041BDBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS2041BDBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS2041BDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS2041BDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2042BDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS2042BDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2042BDRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| TPS2042BDRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| TPS2043BDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TPS2044BDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TPS2051BDBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS2051BDBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS2051BDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS2051BDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|----------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2052BDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS2052BDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2052BDRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| TPS2052BDRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| TPS2053BDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TPS2054BDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|---------------|-----------------|------|------|-------------|------------|-------------|
| TPS2041BDBVR | SOT-23 | DBV | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS2041BDBVT | SOT-23 | DBV | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS2041BDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| TPS2041BDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS2042BDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| TPS2042BDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS2042BDRBR | SON | DRB | 8 | 3000 | 346.0 | 346.0 | 35.0 |
| TPS2042BDRBT | SON | DRB | 8 | 250 | 203.0 | 203.0 | 35.0 |
| TPS2043BDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|---------------|-----------------|------|------|-------------|------------|-------------|
| TPS2044BDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| TPS2051BDBVR | SOT-23 | DBV | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS2051BDBVT | SOT-23 | DBV | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS2051BDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| TPS2051BDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS2052BDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| TPS2052BDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS2052BDRBR | SON | DRB | 8 | 3000 | 346.0 | 346.0 | 35.0 |
| TPS2052BDRBT | SON | DRB | 8 | 250 | 203.0 | 203.0 | 35.0 |
| TPS2053BDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| TPS2054BDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

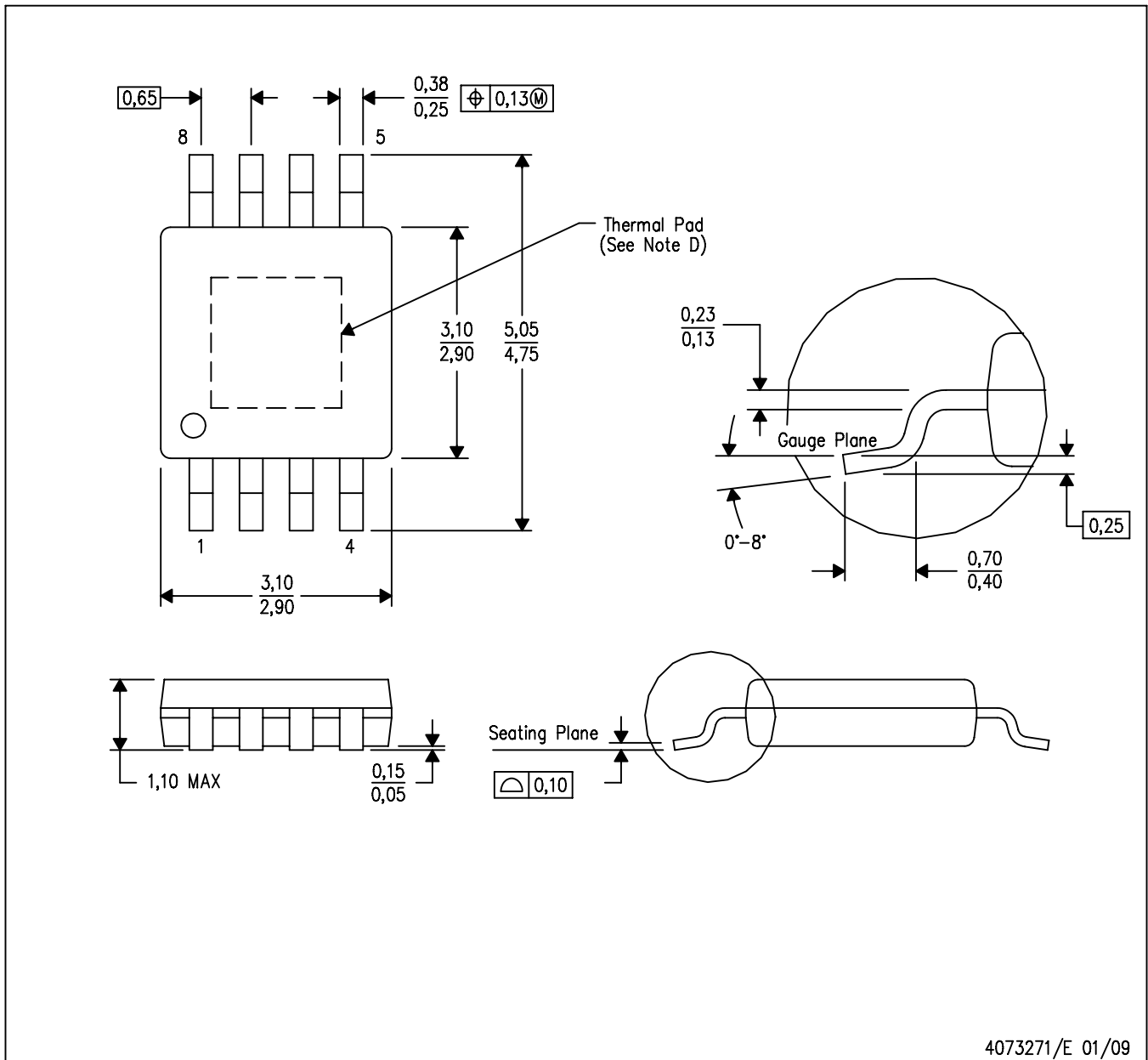


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

MECHANICAL DATA

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. Falls within JEDEC MO-187 variation AA-T

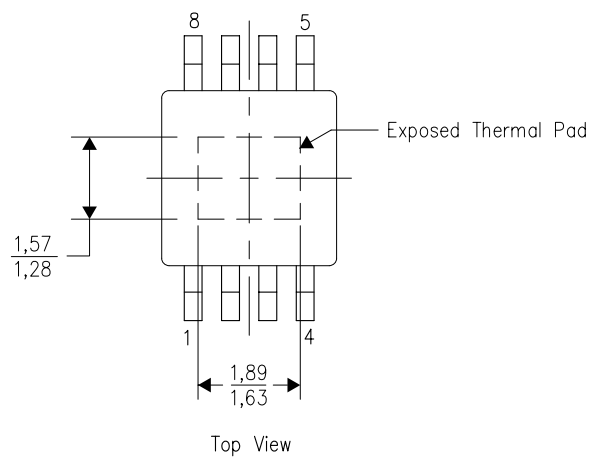
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

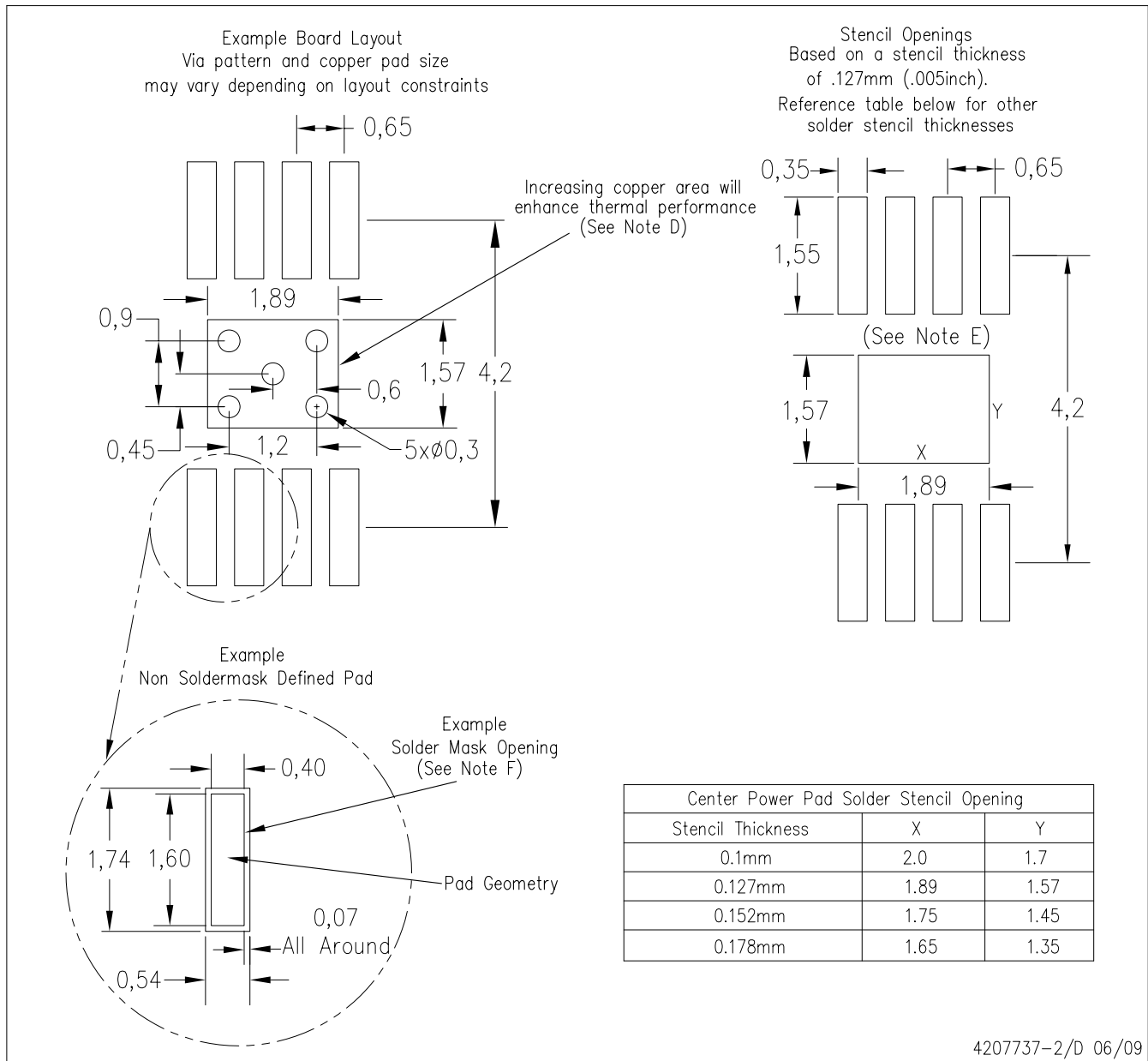
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

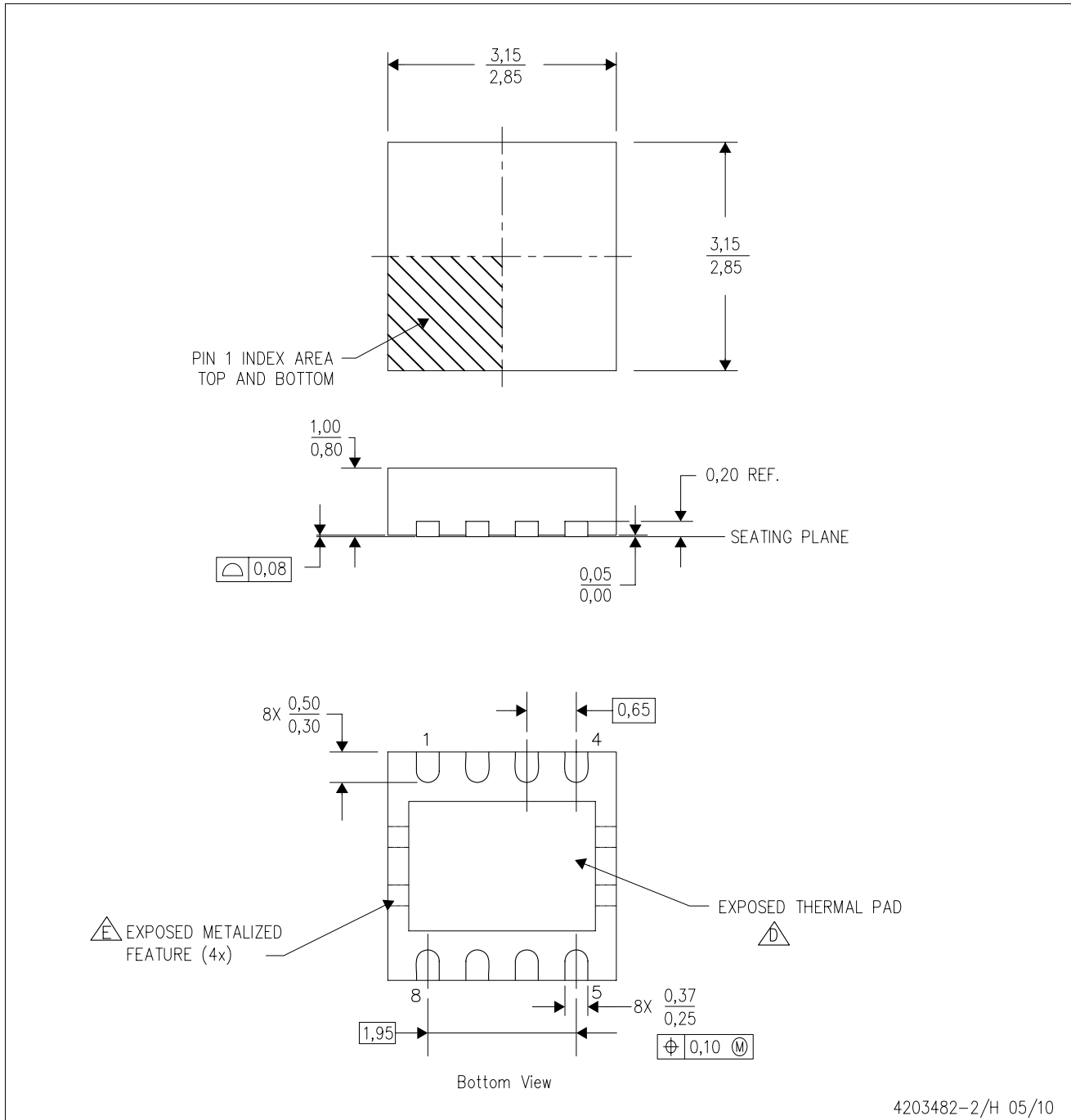
DGN (R-PDS0-G8) PowerPAD™



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

DRB (S-PVSON-N8)

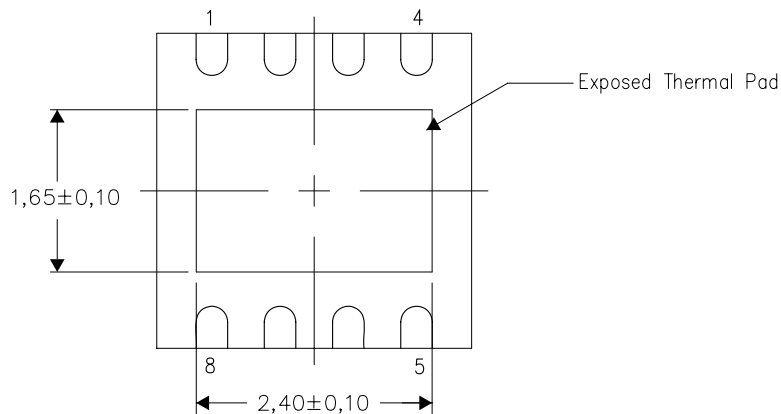
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

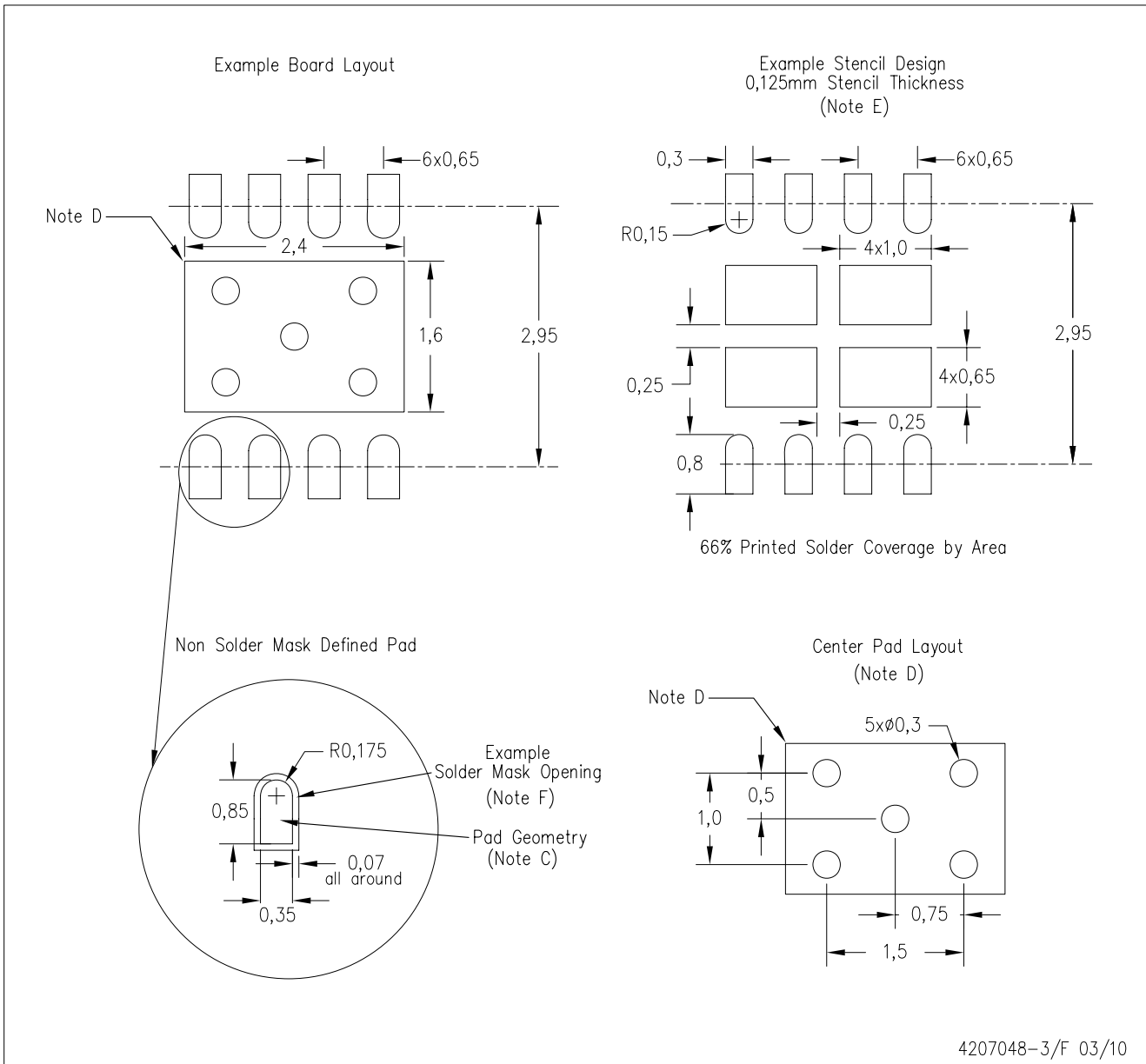
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206340-3/J 07/10

DRB (S-PVSON-N8)

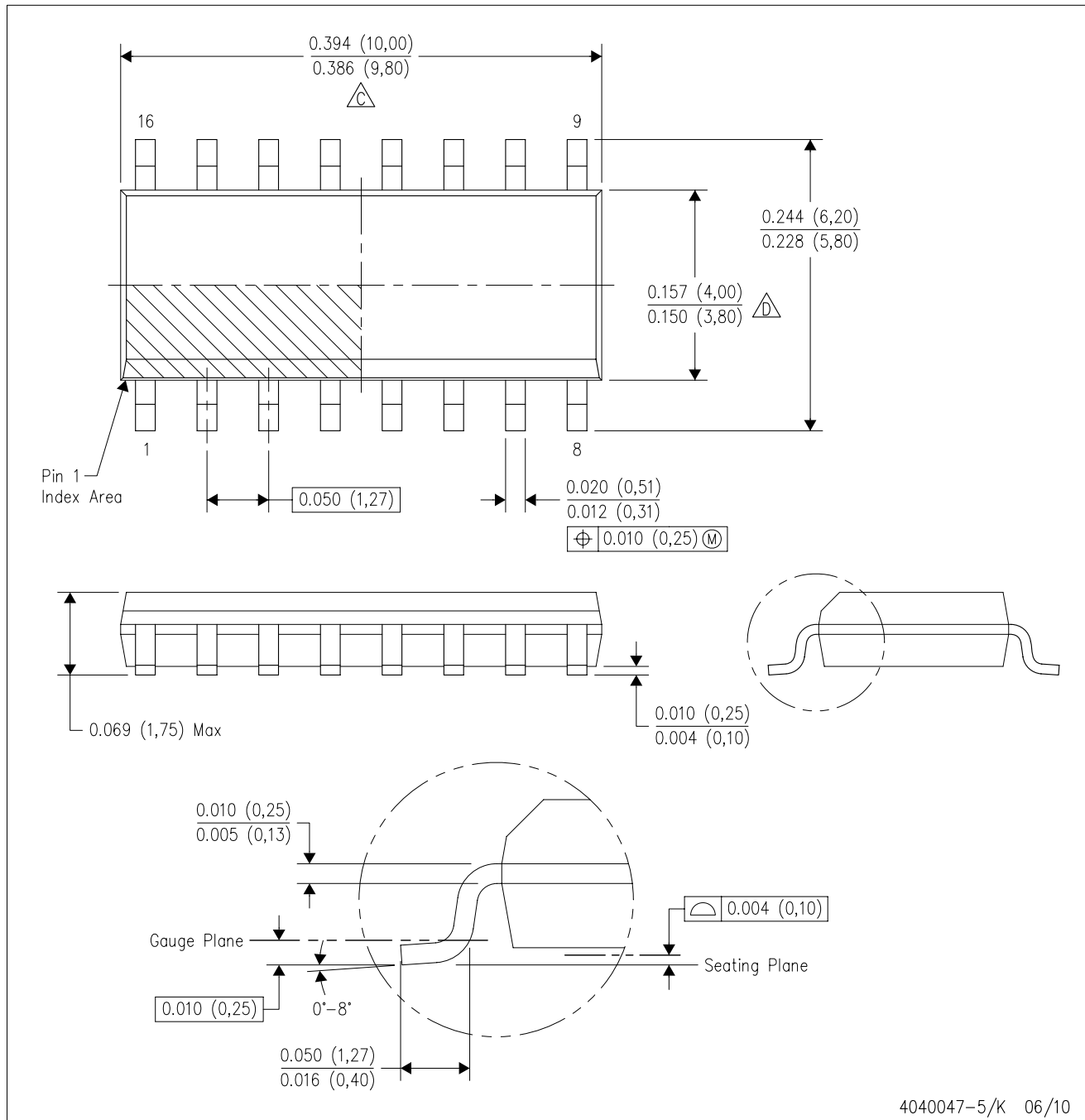
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for solder mask tolerances.

D (R-PDSO-G16)

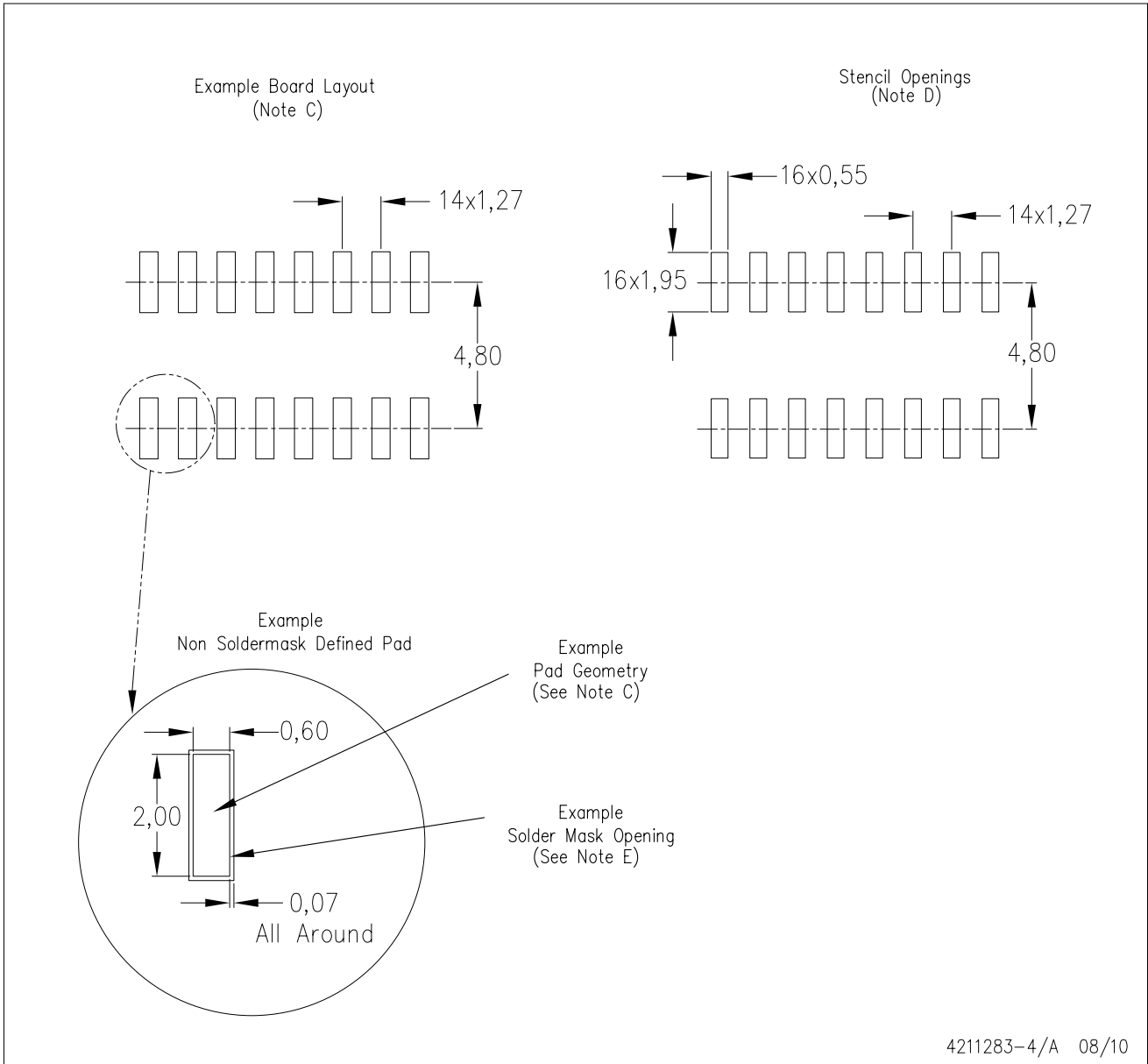
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

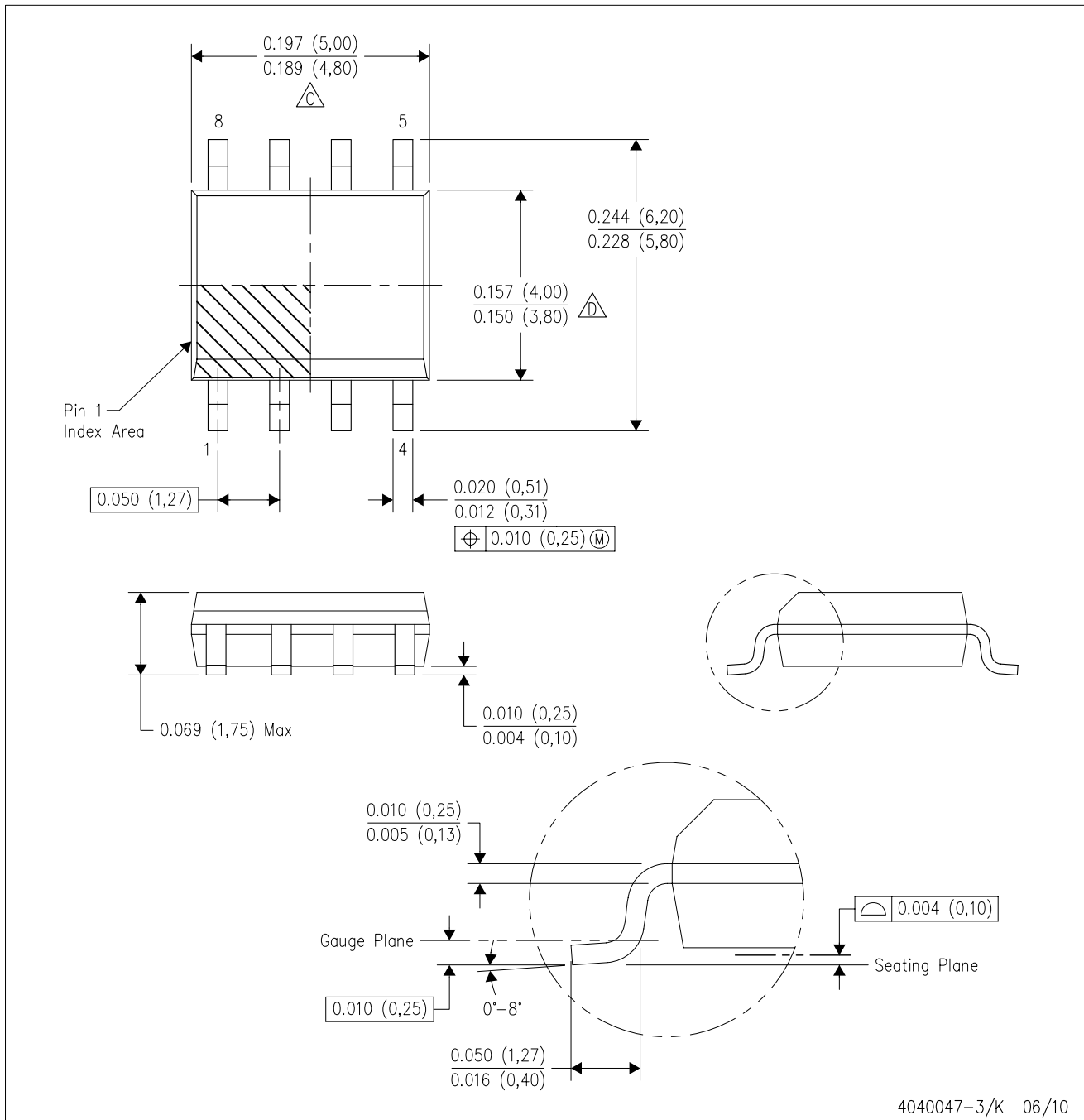
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

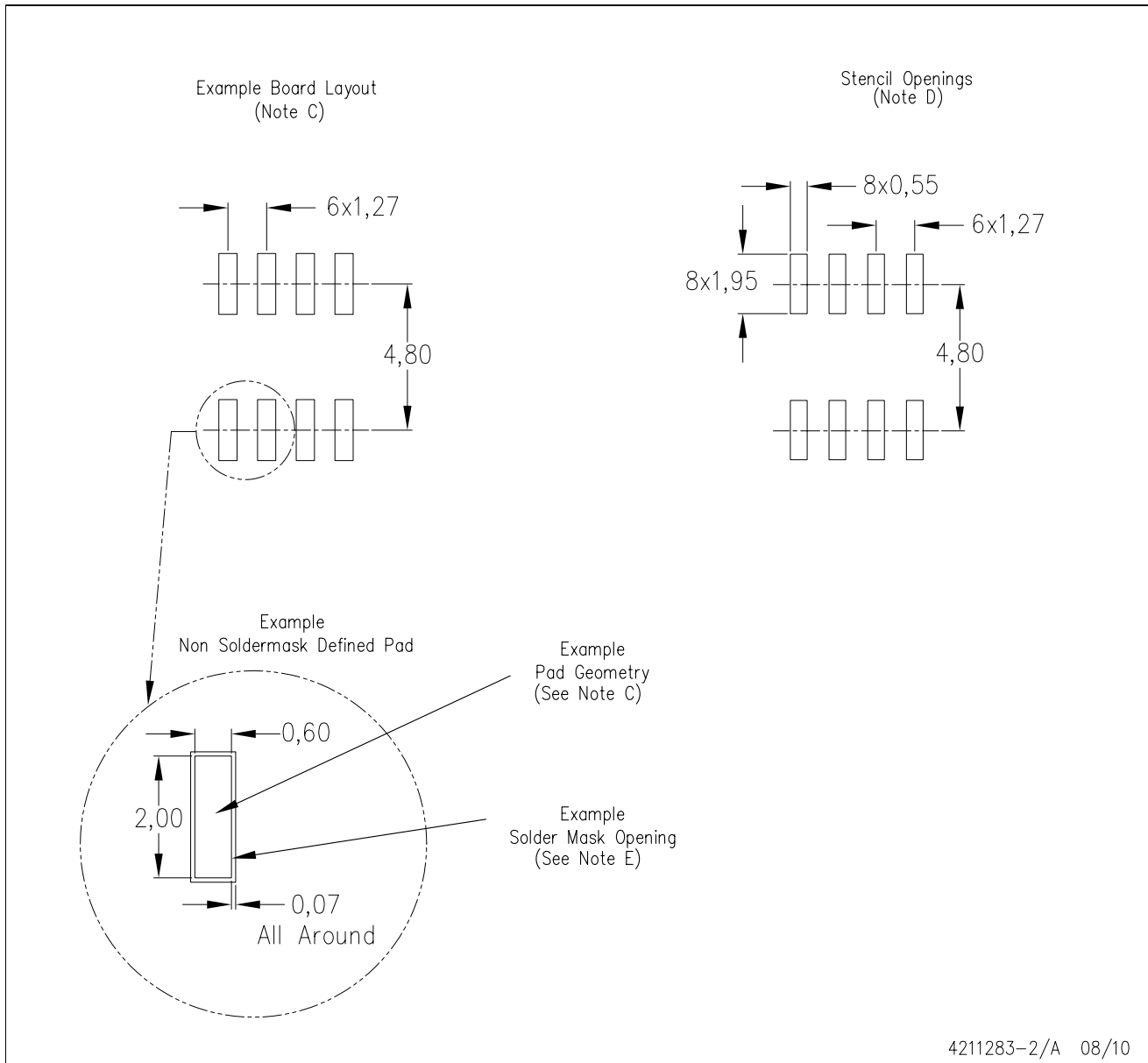
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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